

55LQ3

- 28 Vin DC/DC Converter
- 100 Watts
- Quad Outputs



Features

- High Power Density, Low Profile Packaging
- Full Output Power at +85°C Temperature
- Wedgelock, Plug-in Design
- Designed with component derating Per (NAVSO P3641)
- EMI Filtering Designed to MIL-STD-461
- Remote Sense, Enable and Power Fail Warn
- Transient Protection per MIL-STD-704
- Standard PCI 47 Pin Power Connector & Pinout per PICMG 2.11

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Description

NAI's **55LQ3** is a high power density, low profile, 28VIN DC/DC switch mode converter. The **55LQ3** is ideally suited for cPCI airborne, shipboard and ground applications.

Electrical Specifications

DC Input Characteristics:

Input	16 to 36 VDC; 80 VDC maximum with no damage
EMI/RFI Characteristics	Designed to meet the requirements of MIL-STD-461E; CE102
Input Transient Protection	Per MIL-STD-704

DC Output Characteristics:

Output Power	100 Watts, See Table 2
Output Voltage	See ordering information, output channel codes; sheet 3
Efficiency	75% for typical configuration
Line Regulation	Within 0.1% for low to high line changes at constant load
Load Regulation	0.1% for 0 to 100% of rated load at nominal input line
PARD (Noise and Ripple)	50 mV p-p maximum (20 MHz bandwidth)
Load Transient Recovery	Output voltage returns to regulation limits within 0.5 msec (typical), half to full load
Load Transient Under/Overshoot	0.35 V max from nominal output voltage set point for 3.3 & 5.0 outputs, other outputs 5%.
Short Circuit Protection	Continuous Short circuit protection, with automatic recovery

DC Output Characteristics (Continued):

Current Limiting	120% ±10% typical
OverVoltage Protection	Automatic electronic shutdown if voltage exceeds 125% ±10%
Remote Error Sensing	Compensates for up to 0.5-volt drop on +5vdc, +3.3vdc and +12vdc output leads
Isolation Voltage	500 VDC input to output and input to case; 100 VDC output to case.
Insulation Resistance	50 Megohm at 50 VDC
Signal Types:	
Enable	$V_{IL} = 1V$ max, $V_{IH} = 3V$ min. Input has 1K Pull-down resistor. Floating or Low enables the switched outputs. High will disable the switched outputs.
Power Fail Warning (PFW)	Open collector output capable of sinking 50 mA. Output will be low (conducting) when input is insufficient to produce full power

Physical/Environmental Specifications

Temperature Range	Operating: -55°C to +85°C at 100% load (Temperature measured at card edge); Storage -55°C to +125°C
Temperature Coefficient	0.01% per °C
Shock	30 G's each axis, per MIL-STD-810C, Method 516.2, Procedure 1. Hammer shock per MIL-S-901C
Acceleration	6 G's per MIL-STD-810C, Method 513.2, Procedure 11, and 14 G's per Procedure 1
Vibration	Per MIL-STD-810C, Method 514.2, Procedure 1A
Reliability (MTBF)	500,000 hours, ground benign, at 50°C baseplate
Humidity	95% at 71°C per MIL-STD-810C, Method 507.1 (non-condensing)
Altitude	40,000 feet per MIL-STD-810C, Method 504.1, Category 6 Equipment
Dimensions	See Mechanical Outline; page 5
Salt & Fog	Per MIL-STD-810C, Method 509.1
Sand/Dust/Fungus	Per MIL-STD-810C
Enclosure	Aluminum housing to aluminum baseplate
Finish	Yellow Chemfilm; IAW Mil-C-5541, Class 1A
Interface	Connections per Table 2
Weight	1.25 lbs. max

Table 4 Pinout Designations

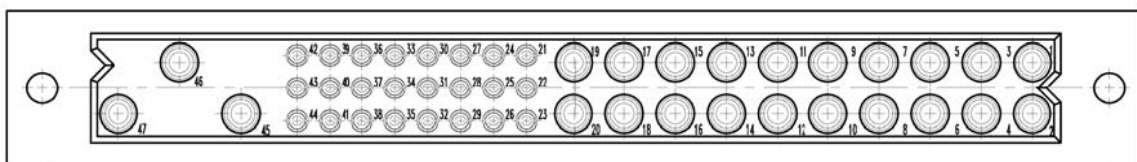
Pin # ⁽¹⁾	Staging # ⁽²⁾	Signal Name	Description
1-4	M	V1	+5vdc Output
5-12	M	RTN	V1 and V2 Return
13-18	M	V2	+3.3Vdc Output
19	M	RTN	V3 Return
20	M	V3	+12vdc Output
21	M	V4	-12Vdc Output
22	M	RTN	Signal Return
23	M	N/C	n/c
24	M	RTN	V4 Return
25	M	N/C	n/c
26	M	N/C	n/c
27	S	EN#	Enable
28	M	N/C	n/c
29	M	N/C	n/c
30	M	V1 SENSE	+5Vdc Remote Sense
31	M	N/C	n/c
32	M	N/C	n/c
33	M	V2 SENSE	+3.3Vdc Remote Sense
34	M	S RTN	Common Sense Return for V1, V2, V3
35	M	N/C	n/c
36	M	V3 SENSE	+12Vdc Remote Sense
37	M	N/C	n/c
38	M	N/C	n/c
39	M	N/C	n/c
40	M	N/C	n/c
41	M	N/C	n/c
42	M	FAL#	PFW (Power Fail Warn)
43	M	N/C	n/c
44	M	N/C	n/c
45	L	CGND	Chassis Ground (safety ground)
46	M	+DC IN	+DC Input
47	M	-DC IN	-DC Input

⁽¹⁾ Pin numbers illustrated are of the female backplane connector

⁽²⁾ L = Long length pins (first mate, last break), M = Medium length pins, S = Short length pins (last mate, first break)

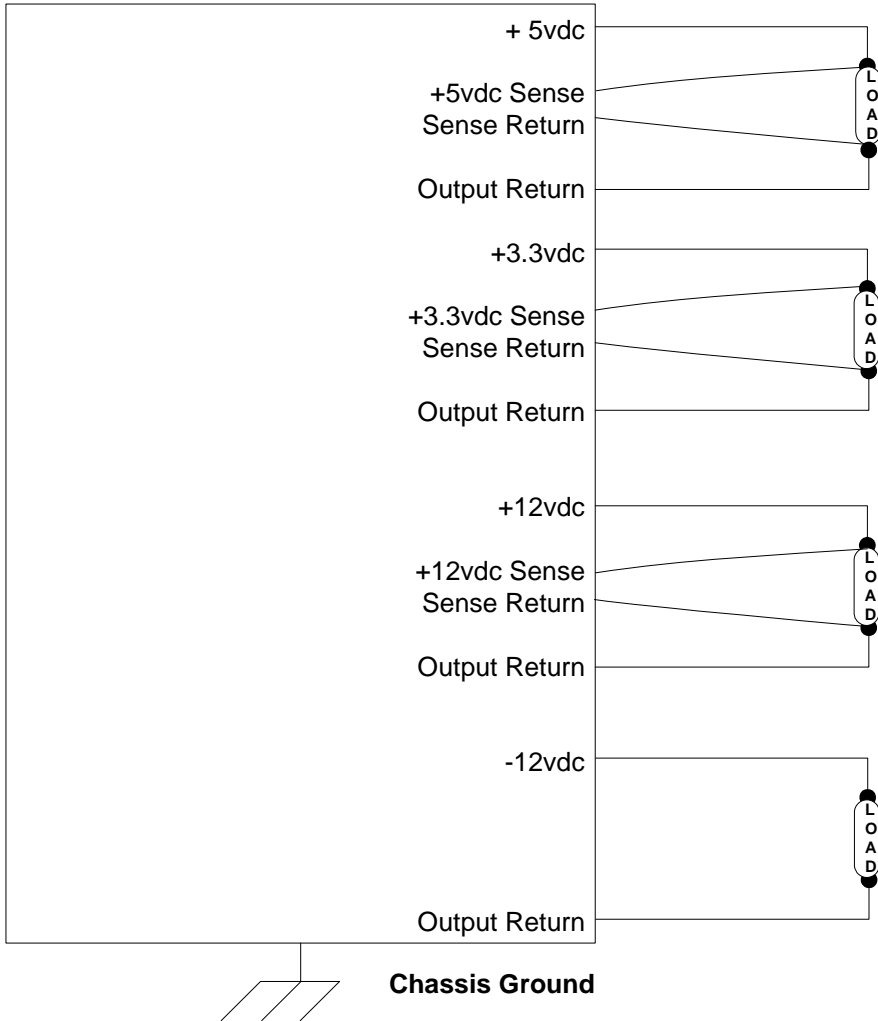
⁽³⁾ These signals are to be defined by PICMG 2.9 Secondary System Management Bus

Connector Positronic PCIH47M400A1



Output Wiring Diagram

55LQ3 Output Example



Mechanical Layout

