data sheet

APX3910-EN

Single Stream STANAG3910
Test & Simulation Module - Rafale
for PCI-X

Avionics Databus Solutions

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product guide

AIM-APX3910-EN

General Features

The APX3910-EN is a member of AIM's new 4th generation family of advanced PCI-X modules for analysing, simulating, monitoring and testing of STANAG3910 databuses.

The APX3910-EN module concurrently acts as Bus Controller, Multiple Remote Terminals (31) and Chronological/ Mailbox Bus Monitor.

The APX3910-EN provides one fully independent STANAG3910 HS bus and Low Speed interface on a single 'Short Length PCI-X' card form factor.

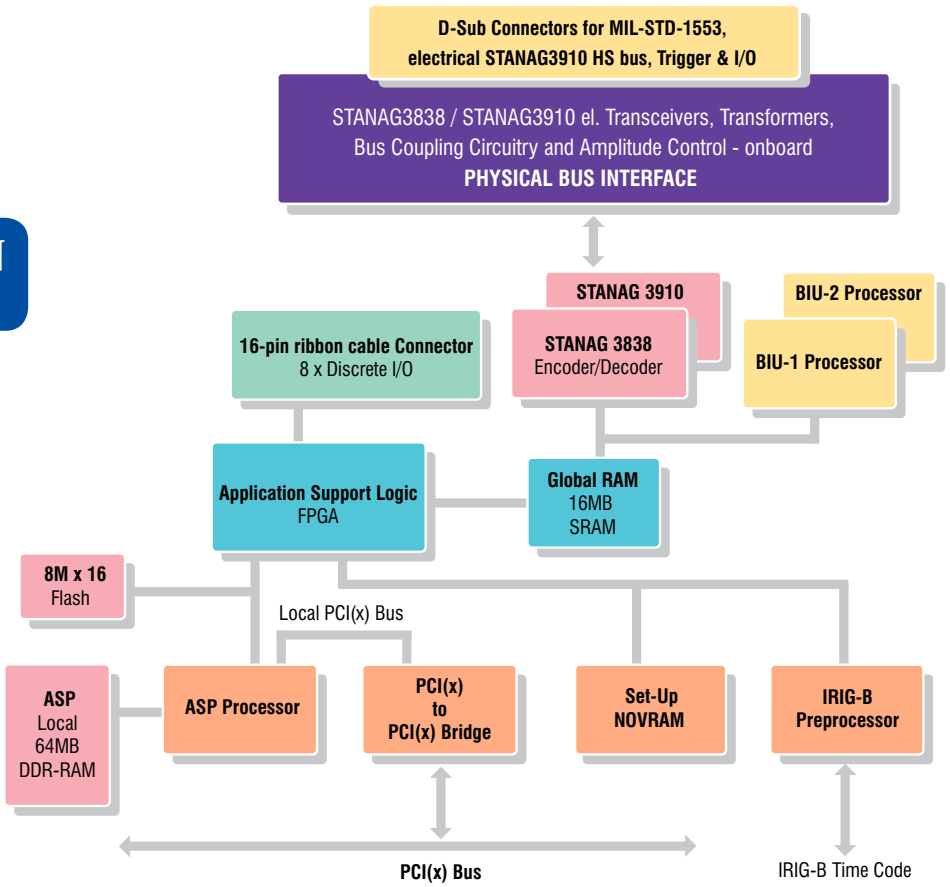
The APX3910-EN can be used for Protocol Testing and Simulation of STANAG3910 LS/ HS Bus Controller, Multiple Remote Terminals and Chronological Monitoring at full bus loads.

All BC/ RT/ BM operations are performed concurrently with no degradation of performance in any operational LS/ HS mode. The APX3910-EN incorporates full protocol error injection and detection and allows the reconstruction and replay of previously recorded electrical STANAG3910 bus traffic to the LS/ HS databus with excellent timing accuracy. The APX3910-EN provides a single PCI-X slot solution with all the databus signals accessible on a single front panel.

The APX3910-EN card uses AIM's Common Core hardware design utilising multiple RISC processors with 16MB of global RAM and 64MB of ASP RAM. An Application Support Processor (ASP) that executes the Driver Software onboard, minimises the load on the host processing system. The onboard processing and large memory provided allows autonomous operation for real time applications and reduces interaction with the host processing system. An IRIG-B time encoder/ decoder that provides both sinusoidal and a free wheeling mode is included for time tag synchronisation at the system level for single or multiple APX3910-EN modules.

Full function driver software is delivered with the APX3910-EN card in a comprehensive Board Software Package (BSP). The optional PBA.pro™ Databus Test & Analysis Tool (for Windows & Linux) can also be purchased for use with the APX3910-EN card. For legacy PBA-3910/ ParaView Databus Analyser/ Visualiser Software (for Windows) please contact the factory.

APX3910-EN
Block Diagram



Bus Controller

The APX3910-EN provides real time Bus Controller (BC) functions for the dual redundant STANAG3910 LS/HS databus system including data buffer queues for generation of dynamic data functions for LS/HS messages.

Key Features of the Bus Controller Mode include:

- *Autonomous operation including sequencing of LS Minor/ Major Frames*
- *Acyclic message insertion/ deletion*
- *Programmable BC Retry without host interaction*
- *Programmable HS Transmitter Initialise Time & HS Receiver Timeout*
- *Full LS/HS Error Injection down to word and bit level*
- *Multi-Buffering with Real Time Data Buffer Updates*
- *Synchronisation of BC operation to external trigger inputs*
- *LS Bus 4µs Inter Message Gaps*

Multiple Remote Terminal

The APX3910-EN can simulate up to 31 LS/HS Remote Terminals with all sub-addresses each providing individually programmable Response Time. Each HS RT simulates all 128 Message Identifiers (MID). LS/HS RT's can be programmed in 'Mailbox Monitor Mode' for non-simulated RT's. The interface provides data buffer queues allowing the generation of dynamic data functions for LS/HS messages.

Key features of the Remote Terminal Simulation Mode include:

- *Programmable Response Time for Each RT with fast RT Response at 4µs*
- *Multi-Buffering for each simulated RT, Sub-Address and MID*
- *Full LS/HS Error Injection for each simulated RT, Sub-Address and MID down to word and bit level*
- *Programmable & Intelligent Response to Mode Codes*
- *Multi-Buffering with Real Time Data Buffer Updates*

Chronological Bus Monitor

The APX3910-EN includes a powerful LS/HS Chronological Bus Monitor and analysis function with multiple trigger and programmable capture capabilities. Accurate time tagging of both LS and HS messages, intermessage gaps, response time and transmitter initialise time is supported. LS/HS messages are time tagged to a 1µs resolution. LS response time and inter message gaps as well as HS transmitter initialise time are measured down to 0.25µs.

Key features of the Chronological Bus Monitor include:

Multi Level Complex Sequence Trigger on:

- *LS/HS Error, LS/HS Word*
- *LS/HS Data Word in Limits*

Monitor and Bus Traffic Capture:

- *16MB of Onboard Memory for LS/HS Messages*
- *Trigger on Start, Centre and End*
- *LS/HS Message Counters*

Physical Bus Replay

The APX3910-EN module can reconstruct previously recorded STANAG3910 databus traffic to both the LS and HS databus simultaneously with excellent timing accuracy. Recorded data files can be selected for Physical Bus Replay. The additional capability to disable any or all RT responses from the STANAG3910 replay enables smart systems integration and test to be performed.

Application Support Processor

The onboard Application Support Processor (ASP) offers processing functions typically provided by the host processor system.

Operational features include:

- *Driver Software Execution onboard*
- *Dynamic Data Generation*
- *Possibility of Customer Specific Programming of the ASP*
- *Runs under Realtime Operating System*

IRIG-B Time Encoder/ Decoder

APX3910-EN modules include an onboard IRIG-B time encoder/ decoder with a sinusoidal output and a free wheeling mode for time tag synchronisation. This allows synchronisation of multiple APX3910-EN cards to one common IRIG-B time input source or to the onboard time code generator of one APX3910-EN card as the reference for the correlation of data across multiple STANAG3910 streams.

Physical Bus Interface

The Physical Bus Interface (PBI) including STANAG3910 HS bus Electrical Front End (EFE) and MIL-STD-1553 transceiver is implemented completely on a single board. Bus Interface Unit (BIU) processors support the encoder/ decoder functions for STANAG3910 and STANAG3838/ MIL-STD-1553A/B protocols.

The APX3910-EN main board also supports both High Speed (HS) and MIL-STD-1553B Low Speed (LS) bus connections including a resistive terminated bus network as well as I/O connections for Front panel Triggering and IRIG-B signals. Coupling to an external data bus system is software programmable.

Driver Software Support

The Driver Software resides on the APX3910-EN module. A full function Application Programming Interface (API) is provided compatible with WindowsXP/Vista/7 and Linux. Host Applications can be written in C and C++.

A LabView VI application interface as well as LabView RT drivers are provided.

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AIM Office Contacts:

AIM GmbH
Sasbacher Str.2
79111 Freiburg
Germany
Tel: +49 761 45 22 90
Fax: +49 761 45 22 93 3
email: sales@aim-online.com

Vertriebsbüro München
Terofalstrasse 23 a
80689 München
Germany
Tel: +49 89 70 92 92 92
Fax: +49 89 70 92 92 94
email: salesgermany@aim-online.com

AIM UK
Cressex Enterprise Centre
Lincoln Road
High Wycombe
Bucks, HP12 3RB
UK
Tel: +44 1494 446844
Fax: +44 1494 449324
email: salesuk@aim-online.com

AIM-USA
Seven Neshaminy Interplex
Suite 211
Trevose
PA 19053
USA
Tel: 267-982-2600
Toll Free: 877-520-1553
Fax: 215-645-1580
email: salesusa@aim-online.com

www.aim-online.com

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Technical Data

Sub-System Interface:
PCI-X Bus Master & Slave, Revision 2.3, 33/66/100/133MHz, 32/64-bit, 5V & 3.3V compatible

Processors:
Two 32-bit 600MHz XScale Processors for MIL-STD-1553 & STANAG3910 BIUs, 32-bit 400MHz Intel IOP for ASP with 64-bit Data Path

Memory:
Global: 16MB S-RAM; ASP: 64MB DDR-RAM

Encoder/Decoder:
STANAG3910/ STANAG3838 Transceiver (TRAFO) with full error injection & detection capability

Time Tagging:
46-bit absolute IRIG-B Time with 1μs resolution, sinusoidal IRIG-B output with free wheeling mode

Physical Bus Interface (PBI):
Physical Bus Interface (PBI) including Electrical Front End (EFE) with the electrical STANAG3910 HS bus signals and STANAG3838 Transceiver (TRAFO); Dual Redundant STANAG3838/ MIL-STD-1553B Transceiver with Variable Output Amplitude, Programmable Bus Coupling modes with onboard terminated Bus Network

Connectors:
STANAG3910 connections:
D-Sub 9-way Connector for the electrical STANAG3910 HS bus signals

STANAG3838/ MIL-STD-1553B connections:
High-Densitiy D-Sub 15-way Connector including STANAG3910/ MIL-STD-1553 TTL-Trigger I/O, RS-232 Maintenance port, IRIG-B Time Code I/O Signals and one General Purpose Discrete I/O Signal

Dimensions: 175mm x 107mm short length PCI format

Power Consumption: 13.5W typical @ +5VDC
2W typical @ +12VDC
0.5W typical @ -12VDC

Operating Temp. Range: Standard 0°C...+45°C. Extended -15°C...+60°C ambient

Storage Temp. Range: -40°C...+85°C ambient

Humidity: 0 to 85% non-condensing

Ordering Information

APX3910-EN
Single Stream, Dual Redundant PCI-X to STANAG3910 Interface:
BC, Multi RT, Mailbox and Chronological Monitor; IRIG-B Time Encoder/ Decoder, 8 General purpose Discrete I/O's (on board-to-board connector); 16MB Global RAM, 64MB ASP RAM; Onboard Electrical Front End (EFE)

Simulator Only Version available:
BC, Multi RT Simulator with Mailbox Monitor

Single Function Version available:
Chronological Monitor and Mailbox Monitor OR Bus Controller OR Multi-RT and Mailbox Monitor

ACB3910-HD15
Ready Made Adapter Cable (2.0m): From 15-pin High Density D-Sub to two Twinax PL75-female Connectors and 15-pin D-Sub Connector for Trigger-I/O, RS-232 Maintenance and IRIG-B Time Code Signals