Model cPCI-78C1 (6U)

A/D, D/A, Discrete I/O, TTL I/O, RTD, Synchro/Resolver and LVDT/RVDT Channels

cPCI bus

MULTI-FUNCTION CARD

A/D, D/A, Discrete I/O, TTL I/O, RTD, Synchro/Resolver and LVDT/RVDT Channels

EXTENSIVE DIAGNOSTICS

COMMERCIAL OR MILITARY TEMPERATURE RANGE

FEATURES

- Multiple functions on a single slot compact PCI (cPCI) card
- No damage if Signals are applied when card is not powered
- Commercial or Severe Environment MIL
- Conducted cooled versions available
- Software Driver/Library and Support Kit available at http://www.naii.com

DESCRIPTION

This universal card eliminates the need for specialized, single function cards by providing an assortment of functions on one single card. The "mother board" contains **6 independent module slots**, each of which can be populated with a function specific module. The available functions are as follows:

Function	Module	Channels	Details
A/D	C1, C2, C4, C3	10	±1.25 to ±50 VDC and 4-20ma versions
D/A	J3, J5, F3, F1	10	±1.25, ±2.5, ±5V, ±10 VDC, Isolated or Non-Isolated versions
	J7	4	High Voltage, ±20 to ±80 VDC, Isolated
Signal Generator	E1	4	Function Generator, 10-130kHz, 0-15Vpp (5.3 Vrms)
Digital I/O	D1	16	TTL (5V System Logic Supply), Programmable for Input or Output
	D2	11	Differential Multi-Mode Transceivers
Discrete I/O	K2, K4	16	Discrete (0-40 VDC), Programmable for Input or Output, Isolated or Non-Isolated
LVDT/D[1]	L	4	LVDT-to-Digital, 2, 3 or 4 wire LVDT and one optional excitation per card
R/D[1]	R2, R3, R4	4	Resolver-to-Digital and one optional reference per card
RTD	G1	6	3 or 4 wire Platinum Resistance Temperature Device Measurement
RVDT/D[1]		4	RVDT-to-Digital and one optional excitation per card
S/D[1]	S1, S2	4	Synchro-to-Digital and one optional reference per card

Note 1: For these functions and other frequency ranges, see 78CS1 and/or contact factory.

Automatic background BIT testing, an important feature, is always enabled and continually checks the health of each channel. There is no need to guess or make assumptions about system performance. A fault is immediately reported and the specific channel is identified. This capability is of tremendous benefit because it identifies and reports a failure, without the need to shut down the equipment for troubleshooting. Testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card and can be disabled on a per channel basis. (See Operational Instructions for further detail within this specification.)

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SPECIFICATIONS

General	**For the Carrier Card (Mother Board)**
Signal Logic Level:	Automatically supports either 5V or 3.3V PCI bus.
Power (Mother board):	+5 VDC at 460mA and ±12V at 15mA, then add power for each individual module.
Temperature, operating:	"C" =0°C to +70°C, "E" =-40°C to +85°C (see part number)
Storage temperature:	-55°C to +105°C
Temperature cycling:	Each board is cycled from -40°C to +85°C for 24 hrs, option “E” or “H” (see part number)
Size:	6U (9.2") height, 4HP (0.8") width. 233.4 mm x 20.3 mm x 160 mm deep
Weight:	16 oz. (454g) unpopulated. add weight for each module (typically 1 oz. each) add 2 oz. (57g) for reference supply add 2 oz. (57g) for wedgelocks

A/D (Module C1)	**Ten (10) A/D (1.25 VDC to 10.0 VDC FS) Uni or bipolar**
Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as F.S. inputs of: 10.00, 5.00, 2.50, or 1.25 volts where range is ±FS or 0 to FS VDC. The ability to set lower voltages for Full Scale, assures the utilization of the full resolution.
Over-voltage.	No damage up to ±12 V continuous; ±30 V momentary
Open Input sense:	This module will sense and report unconnected Inputs
Input Impedance:	1 MΩ min.
Accuracy:	0.05 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB’s max. over temperature
Sampling rate:	50 KHz per channel
Band Width:	20 KHz
Group delay:	770 microseconds (time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz
Common mode voltage:	Signal voltage plus Common mode equals 10.5 volts
Output Logic:	Bipolar output in two's complement. 7FFF is max. positive, 8000 is max. negative. Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns.
Power:	±12 VDC at 25ma typical, 50 ma max As of 4/5/05, no ±12 VDC requirement. +5 VDC at 320 ma typical, 500 ma max. As of 4/5/05, 500ma typical, 750ma max.
Weight:	1 oz. (28g)

A/D (Module C2)	**Ten (10) A/D (40VDC) Uni or bipolar**
Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as full scale inputs of: 40.00, 20.00, 10.00, or 5.00 volts where range is ±FS or 0 to FS VDC. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution. This module will not sense open Inputs
Over-voltage protected:	±100 Volts
Input Impedance:	500 kΩ min. (Differential)
Accuracy:	0.1 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB’s max. over temperature
Sampling rate:	50 KHz per channel
Band width:	20 KHz per channel
Group delay:	770 microseconds (Time for data sample to propagate to data register)

Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz
Output Logic:	Bipolar output in two's complement. 7FFF is max. positive, 8000 is max. negative. Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 25ma typical, 50 ma max As of 4/5/05, no ±12 VDC requirement. +5 VDC at 320 ma typical, 500 ma max. As of 4/5/05, 500ma typical, 750ma max.
Weight:	1 oz. (28g)

A/D (Module C3) **Ten (10) 4-20ma Current Measurement Module**

Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input, 0-25ma)
Input scaling:	Ten (10) unipolar channels, 0-25ma full scale. This module will not sense open Inputs
Input voltage:	Not to exceed ±3 volts.
Input Impedance:	100 Ω min.
Accuracy:	0.1 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±8 LSB's max. over temperature
Sampling rate:	50 l per channel
Band width:	20 l per channel
Group delay:	770 microseconds (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 l in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 l
Common mode voltage:	Signal voltage plus Common mode equals 80 volts
Output Logic:	Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 25ma typical, 50 ma max As of 4/5/05, no ±12 VDC requirement. +5 VDC at 320 ma typical, 500 ma max. As of 4/5/05, 500ma typical, 750ma max.
Weight:	1 oz. (28g)

A/D (Module C4) **Ten (10) A/D (50VDC) Uni or bipolar**

Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as full scale inputs of: 50.00, 25.00, 12.50, or 6.25 volts where range is ±FS or 0 to FS VDC. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution. This module will not sense open Inputs
Over-voltage protected:	±100 Volts
Input Impedance:	500 kΩ min. (Differential)
Accuracy:	0.1 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB's max. over temperature
Sampling rate:	50 l per channel
Band width:	20 l per channel
Group delay:	770 microseconds (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 l in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 l
Common mode voltage:	Signal voltage plus Common mode equals 80 volts
Output Logic:	Bipolar output in two's complement. 7FFF is max. positive, 8000 is max. negative. Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 25ma typical, 50 ma max As of 4/5/05, no ±12 VDC requirement. +5 VDC at 320 ma typical, 500 ma max. As of 4/5/05, 500ma typical, 750ma max.

Weight:	1 oz. (28g)

I/O (Module D1) **Sixteen (16) TTL, Programmable for Input or Output**

TTL Input

Input levels:	TTL and CMOS compatible, single ended inputs Each channel incorporates a 100 KΩ pull-down resistor
	$V_{in\ L}$: 0.8 V = "0"
	$V_{in\ H}$: 2.0 V = "1"
	$V_{in\ max.}$: 5.0 V
	I_{IN} = ± 50μA
Read Delay:	1.02 μseconds
De-bounce:	Programmable per bit from 0 to 255 microseconds. LSB= 1 microsecond.

TTL Output

Output levels:	TTL/CMOS, single ended outputs
Drive Capability:	$V_{out\ L}$: +0.5 V max. sink 32 mA max. $V_{out\ H}$: 3.8 V min. source -32 mA max.
Output current:	Channel will withstand a current of 50ma for 4 microseconds and will then be turned off.
Rise/Fall time:	10 ns into a 50pf load
Write Delay:	1.02 μseconds
Power:	+5 VDC System Logic Supply, at 40mA per module
Weight:	1 oz. (28g)

I/O (Module D2) **Eleven (11) Differential Multi-Mode Transceivers**

Mode of Operation:	422 (Differential)	485 (Differential)
Input		
Receiver Input Levels:	-10V to +10V	-7V to +12V
Receiver Input Resistance:	120Ω	>12kΩ
Receiver Input Sensitivity:	±200mV	±200mV
	(Each channel incorporates a 120 Ω termination resistor that can be programmed on a channel by channel basis)	
Read Delay:	1.02 μseconds	
Filtering	1-128, μseconds programmable	
Output		
Driver Output Voltage:	-0.25V to +6V max.	-0.25V to +6V max.
Driver Output Signal Level (Loaded minimum)	±2V	±1.5V
Driver Output Signal Level (Unloaded maximum)	±6V	±6V
Driver Load Impedance:	100Ω	54Ω
Max. Driver Current in Hi Z State (Power ON):	N/A	±100μA
Max. Driver Current in Hi Z State (Power OFF):	±100μA	±100μA
Write Delay:	1.02 μseconds	
Protection:	Short circuit protected, Thermal shutdown, Built-in current limiting	
Rise/Fall time:	31 ns into a 50pf load	
Power (Per 11 channel module):	+5VDC at 1Watt quiescent, 1.8Watts fully loaded (54Ω load per channel)	
Weight:	1 oz. (28g)	

Signal (Module E1) **Four (4) Programmable Frequency Generators**

Output Signal:	Sine, Triangular, or Square Wave, one per channel
Output Frequency:	10 – 130kHz with 1Hz resolution

Output Voltage:	0 – 10Volts peak (7.07Vrms), Programmable, per channel
Accuracy	± 6% FS volts, for frequencies <100Hz ± 1% FS volts, 100Hz – 20kHz ± 6% FS volts, for frequencies >20kHz
Load:	600 ohms min.
Regulation:	7% max. No load to full load.
Phase:	0 – 359.912 ±1% with 0.088° resolution, relative to channel 1. Default is 0.
Power:	+5 VDC at 0.6A per module
Weight:	1 oz. (28g)

D/A (Module F1) **Ten (10) D/A Outputs ±10 VDC, cPCI ISOLATED**

Output range:	±10 VDC or 0 to 10 VDC, programmable. For other ranges contact customer service. Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Non-linearity:	0.01% FS over temperature
Gain error:	0.02% over temperature
Output format:	Optically isolated in groups of ten (250 V to CPCI power)
Settling time:	10 μs max
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	20 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g)

D/A (Module F3) **Ten (10) D/A Outputs ±5 VDC, cPCI ISOLATED**

Output range:	±5 VDC or 0 to 5 VDC, programmable. For other ranges contact customer service. Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Non-linearity:	0.01% FS over temperature
Gain error:	0.02% over temperature
Output format:	Optically isolated in groups of ten (250 V to cPCI power)
Settling time:	10 μs max
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	20 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g)

RTD (Module G1) **Six (6) four-wire Platinum RTD**

Resolution:	16 bits
RTD Interface:	Interfaces with 100Ω and 500Ω RTDs, or any RTD whose operating resistance is up to 2000Ω under the required operating conditions.

Open Input sense:	This module will sense unconnected Inputs. Only one open wire out of four will set flag
Excitation:	1 milliamp/channel
Accuracy:	0.8Ω for 2kΩ range, over temperature and with a 3.75 Hz bandwidth 0.27Ω for 655Ω range, over temperature and with a 3.75 Hz bandwidth
Grounds:	Each input has a separate return, but all are common and connected to cPCI ground.
Update rate:	Each channel is updated seven times per second
Output Format:	Resistance
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns.
Power:	+ 12 VDC at 25 ma typical 50 ma max. +5 VDC at 320 ma typical, 500 ma max
Weight:	1 oz.

D/A (Module J3): Ten (10) D/A Outputs ±1.25 VDC, cPCI ISOLATED

Output range:	±1.25 VDC or 0 to +1.25 VDC, programmable. For other ranges contact factory Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Output format:	Optically isolated in groups of ten (250 V to cPCI power)
Settling time:	350 μs max.
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. 5 KΩ min. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	20 microseconds/channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns.
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max.
Weight:	1 oz. (28g)

D/A (Module J5) Ten (10) D/A Outputs ±2.5 VDC, cPCI ISOLATED

Output range:	±2.5 VDC or 0 to +2.5 VDC, programmable. For other ranges contact factory Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Output format:	Optically isolated in groups of ten (250 V to cPCI power)
Settling time:	350 μs max
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. 5 KΩ min. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	20 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g)

D/A (Module J7) Four (4) D/A Outputs ±20 to ±80 VDC, cPCI ISOLATED

Output range:	±20 to ±80 VDC. Output is set to 0 at reset or Power-on, Programmable in pairs, from ±20V to ±80V.
Returns:	Each D/A return has separate pins that are common within each module. These returns are isolated from cPCI ground

Resolution:	12 bits/channel
Accuracy:	0.15% FS
Settling time:	10 µs
Load:	10 ma/channel max.(Source or Sink). Up to 80VDC. Output current reduced up to 90VDC. Short circuit protected.
Output impedance:	<1 Ω
Update rate:	10 microseconds per channel
Output control:	via software Enable/Disable of DC/DC converter.
Power:	+5 VDC, 250ma max per module
Weight:	1 oz. (28g)

I/O (Module K2) **Sixteen (16) Discrete, ISOLATED, Programmable for Input or Output**

Discrete Input

Input Range:	0 to +40 VDC. User provided Vcc must be greater than or equal to any input signal or current limited to 10ma.
Input Pulse Detection:	A signal pulse width 40µs or greater will be sense and indicated by the appropriate Hi–Lo or Lo-Hi Transition Interrupt
Input Impedance:	40kΩ
Switching Threshold:	Four levels are programmable from 0 to 40 VDC with 10-bit resolution (0.98% FS) On, Off. Short to +V, Short to ground.
Accuracy of Set Point:	The greater of 5% signal value or 0.25 volts
ON/OFF Differential	0.25 V minimum recommended
Voltage/Contact Sensing:	Software selectable per bit.
De-bounce:	Programmable per bit from 0 to 0.655 seconds. LSB= 20 microseconds.
Update Rate:	Each channel is updated every 20 microseconds
Over-Voltage Protection:	to 40 VDC

Discrete Output

Output Range:	+0 VDC to +40 VDC output logic as defined by user provided Vcc input voltage (≥ 8 volts) to that channel bank. There are four channels per bank. For +5V applications use module D1.
Output Current:	0.5 A max. Short circuit protected. **Total current per module not to exceed 2 A.** Channel will withstand a current of 0.75A for 80µs and will then be turned off.
Output Load:	Directly drive inductive loads (relays); Reverse current protection diode is incorporated.
Output Format:	Low-side switched, high-side switched or push-pull. Programmable per bit
Write Delay:	20 µs
Update Rate:	Each channel is updated every 20 microseconds
Over-Voltage Protection:	to 40 VDC
Thermal protection	is provided
Power (Per 16 channel module):	+5VDC at 0.073 A typical, 0.103 A max. For contact sensing add +Vcc: 1.24 x Iset+ (Vcc x 16)/38000
Weight:	1 oz. (28g)

Signal Power

Vcc	4 Vcc input pins per module, each powers an individual 4 channel bank. Vcc ≥ 8 volts. For +5V applications use module D1.
Ground	4 Ground inputs pins per module. All Grounds inputs are common, but isolated from cPCI ground.

Isolation

Vcc-to-cPCI Ground	500 volts
Module-to-cPCI Power	500 volts
I/O Signal	500 volts, Digital I/O is opto-isolated from cPCI bus

I/O (Module K4) **Sixteen (16) Discrete, NON-ISOLATED, Programmable for Input or Output**

Same as Module K2: Except is NON-ISOLATED (where all grounds are tied to cPCI ground)

R/D (Module R2) **Four (4) 400Hz Resolver Measurement**

Same as Module S1 Except:

Input format: Resolver

Input voltage:	Resolver: 11.8V_{L-L}, Transformer isolated
Reference Input:	11.8 Vrms, Transformer isolated.
Bandwidth:	40Hz
Frequency Input:	400Hz

R/D (Module R3)	**Four (4) 400Hz Resolver Measurement**
Same as Module S1	Except:
Input format:	Resolver
Input voltage:	Resolver: 2-28V_{L-L}, Transformer isolated
Reference Input:	2-28 Vrms, Transformer isolated.
Bandwidth:	40Hz
Frequency Input:	400Hz

R/D (Module R4)	**Four (4) 1200Hz Resolver Measurement**
Same as Module S1	Except:
Input format:	Resolver
Input voltage:	Resolver: 11.8V_{L-L}, Transformer isolated
Reference Input:	26 Vrms, Transformer isolated.
Bandwidth:	100Hz
Frequency Input:	1200Hz

S/D (Module S1)	**Four (4) 400Hz Synchro Measurement**
Resolution:	16 bits (up to 24 bits for two-speed configuration)
Accuracy:	±1 arc-minute for single speed inputs ±1 arc-minute divided by the gear ratio for two-speed inputs
cPCI Data transfer:	Data transfers within 200 ns.
Tracking Rate:	150 RPS (Referred to the Fine input for two-speed configuration)
Bandwidth:	40 Hz
Input format:	Synchro
Input voltage:	Synchro: 90V_{L-L}, Transformer isolated
Input Impedance:	100 kΩ min. at 90V_{L-L}
Reference Input:	115 Vrms, Transformer isolated.
Reference Zin	100 kΩ min.
Frequency Input:	400Hz ±40Hz
Angle change alert:	Each channel can be set to a different angle differential. When that differential is exceeded, an interrupt (if enabled) is triggered. Default: “Ch. Disabled”. MSB=180°; Min. differential is 0.05°. Max differential that can be programmed is 179.9°.
Phase shift:	The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°.
Velocity, Digital:	16-bit resolution; Linearity: 0.1%. Scalable to 0.1°/sec resolution.
Wrap around Self Test:	The three different powerful test methods are detailed in the Description section and further described in the Programming Instructions.
Power:	+ 5 VDC: 0.02A ±12 VDC: 0.02A
Weight:	1 oz. (28g)

Reference Supply	**Include as Required**
Voltage:	2.0-28Vrms programmable, resolution 0.1Vrms, or 115Vrms Fixed.
Accuracy:	±2%
Frequency:	360Hz to 10kHz ±1% with 1Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	5VA max. @ 40° min. inductive; 190mA RMS @ 2-26VAC or 45mA RMS @ 115VAC Note: Power is reduced linearly as the Reference Voltage.
Power Dissipation:	1A @ 5VA Load (3A peak)
Weight:	2 oz. (28g)

S/D (Module S2)	**Four (4) 60-400Hz Synchro Measurement**
Same as Module S1	Except:
Tracking Rate:	13.5 RPS for 60-400Hz (Referred to the Fine input for two-speed configuration)
Bandwidth:	10 Hz
Frequency Input:	47-400Hz

ADDRESS CONFIGURATION

This section provides programmers the information needed for developing drivers other than those supplied.

The following information resides in the PCI configuration registers:

Device ID	= 7891	(hex)
Vendor ID	= 15AC	(hex)
Rev	= 01	(hex)
Subsystem ID	= 000115AC	(hex)

Base Address	= Assigned by the PCI BIOS. Interrogate the PCI BIOS for this information.
Required Address space	= 4 for each card.

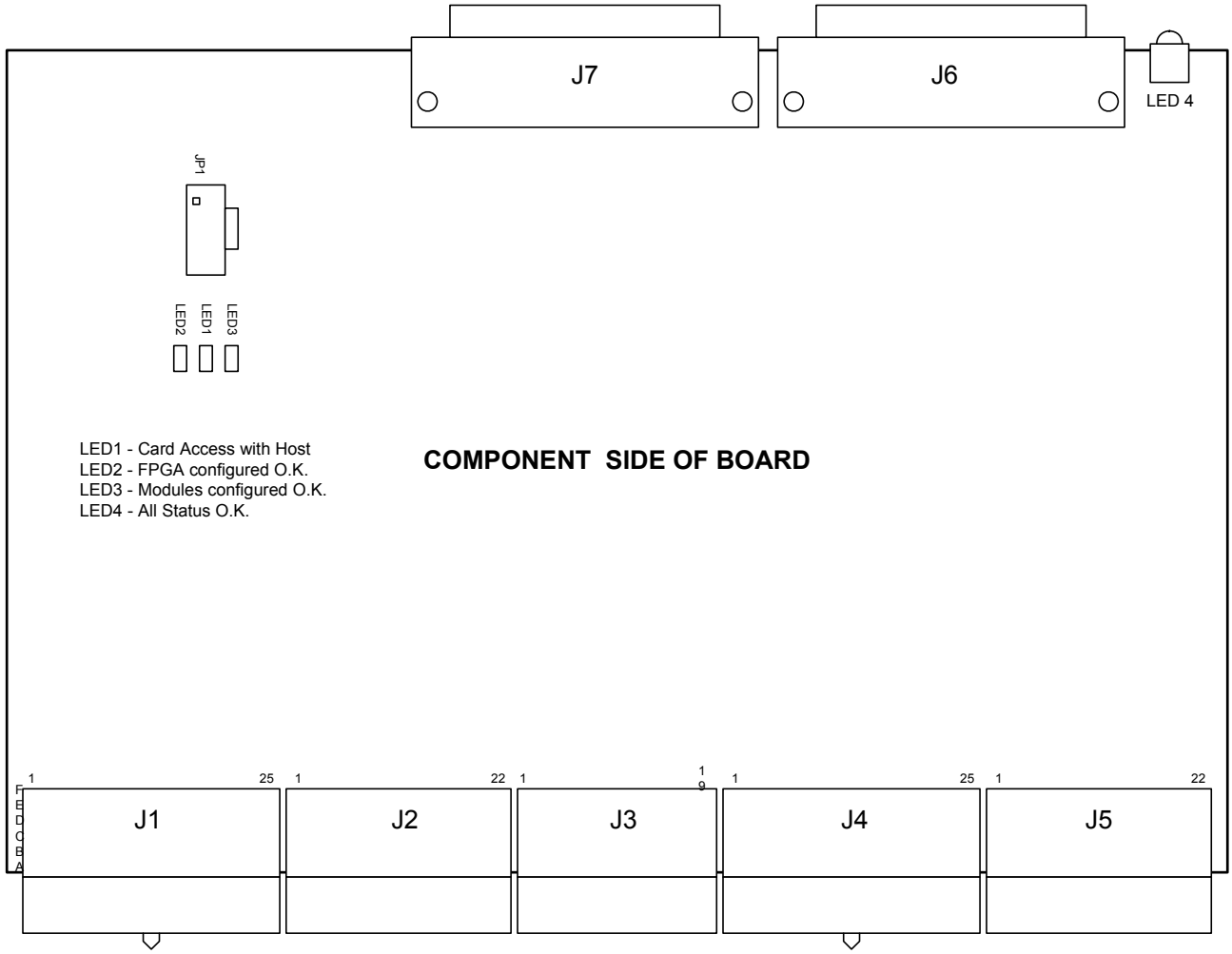


FIGURE 1.

PRODUCT CONFIGURATION AND MEMORY MAP

This design provides multiple functions on a single cPCI (6U) card. When ordering, the customer selects an assortment of up to 6 modules to populate this 6-slot "mother board." The memory map follows the order of modules specified in the part number.

To address the register of any module, use the *Base* address to the entire card, add the *Module Offset* depending upon its slot (000, 200, 400,…or A00), and then add the *Register Offset* of interest (see module memory map.) The memory map of each selected module counts from, or is superimposed over its respective module offset. Thus, **Address = Base + Module Offset + Register Offset**.

For example, if a Digital I/O module were selected to populate module 1 and a Discrete I/O module were selected to populate module 4:

Address = Base + Module 1 Offset 000 + Digital I/O register 010 = Base + 010 hex
Address = Base + Module 4 Offset 600 + Discrete I/O register 024 = Base + 624 hex.

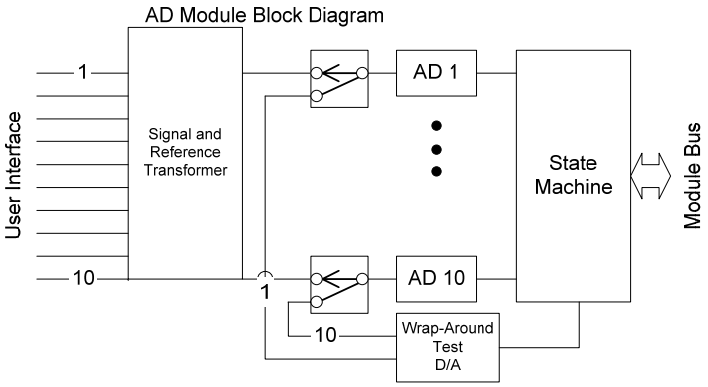
MEMORY MAP

000	Module 1 Register…	400	Module 3 Register…	800	Module 5 Register…
004		404		804	
008		408		808	
00C		40C		80C	
010	Module 1	410	Module 3	810	Module 5
.	Offset 000	.	Offset 400	.	Offset 800
.		.		.	
.		.		.	
1F8		5F8		9F8	
1FC		5FC		9FC	

200	Module 2 Register…	600	Module 4 Register…	A00	Module 6 Register…
204		604		A04	
208		608		A08	
20C		60C		A0C	
210	Module 2	610	Module 4	A10	Module 6
.	Offset 200	.	Offset 600	.	Offset A00
.		.		.	
.		.		.	
3F8		7F8		BF8	
3FC		7FC		BFC	

The memory map of each module type is described hereafter:

A/D (MODULE C)



A/D channels use individual A/D converters with a high (50 kHz) sampling rate per channel. The input range and gain is field programmable for each channel. Each of these differential channels includes a second order anti-aliasing filter and a post filter that has a digitally programmable break point that enables user to field adjust the filtering for each channel. All A/D channels are self-calibrating because each channel, on a rotating basis, is automatically calibrated to eliminate offset and gain errors. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution (does not apply to Current Measurement Module C3 which is fixed unipolar, 0-25mA FS). Open inputs cannot be sensed because scaling input resistor networks are used. All inputs are double buffered for immediate availability. The "Latch" feature permits the user to read all A/D channels at the same time.

The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 0.2% FS. Any failure triggers an Interrupt (if enabled) with the results available in BIT status register. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

In addition, all channels are monitored for open input (except for Current Measurement Module C3 applications).

The (D3) test starts an initiated BIT test that disconnects all A/D's from the I/O and then connects them across an internal stimulus. Each channel will be checked to a test accuracy of 0.2% FS and monitored for open inputs. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from "1" to "0". The test can be stopped at any time and requires no user programming and can be enabled or disabled via the bus.

A (D0) test is used to check the card and cPCI interface. Write "1" to D0 of *Test enable* register to disconnect all A/D channels from the I/O and connects them across an internal D/A. Test parameters are controlled by the user and are entered in the *D0 Test Voltage* and *DO Test Range* registers. The outputs from the A/D channels are monitored by an internal D/A for proper conversion. External reference voltage is not required

A/D Open Circuit monitoring is disabled during D3 testing.

MODULE MEMORY MAP

000	Data 1	R	028	Range & Polarity[1] 1	R/W	050	Filter Break Freq. 1	R/W	18C	Module Design Version[2]	R
004	Data 2	R	02C	Range & Polarity 2	R/W	054	Filter Break Freq. 2	R/W	190	Module Design Revision[2]	R
008	Data 3	R	030	Range & Polarity 3	R/W	058	Filter Break Freq. 3	R/W	194	Module DSP[2]	R
00C	Data 4	R	034	Range & Polarity 4	R/W	05C	Filter Break Freq. 4	R/W	198	Module FPGA[2]	R
010	Data 5	R	038	Range & Polarity 5	R/W	060	Filter Break Freq. 5	R/W	19C	Module ID	R
014	Data 6	R	03C	Range & Polarity 6	R/W	064	Filter Break Freq. 6	R/W	1A0	BIT Status Ch.1-10	R
018	Data 7	R	040	Range & Polarity 7	R/W	068	Filter Break Freq. 7	R/W	1A4	Open Status[3] Ch.1-10	R
01C	Data 8	R	044	Range & Polarity 8	R/W	06C	Filter Break Freq. 8	R/W	1C0	BIT Stat Interrupt Enable Ch.1-10	R/W
020	Data 9	R	048	Range & Polarity 9	R/W	070	Filter Break Freq. 9	R/W	1D4	Open Stat INTR Enable Ch.1-10	R/W
024	Data 10	R	04C	Range & Polarity 10	R/W	074	Filter Break Freq. 10	R/W			

Note: 1. Range & Polarity Register is simply called Range Register in software driver/library.
Range & Polarity does not apply to Current Measurement Module C3
2. Pending.
3. Open Status does NOT apply to High Voltage (20V to 80V), or Current Measurement modules.

Data Read

Two's complement format for bipolar mode; 7FFFh=+FS, 8,000h=-FS. For unipolar mode, range is from 0h to FFFFh = FS.

A/D Range & Polarity

Format input for range and polarity. Range is dependent upon Module. Encode range using data bits D0 through D3. Program polarity using data bit D4. Enter per table. Does not apply to Current Measurement Module (C3 is fixed unipolar, 0-25mA FS).

REGISTER	D15	D1	D1	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RANGE & POLARITY	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**

MODULE	C4	C2	C1					
Unipolar RANGE	0 – 50.0 V	0 – 40.0 V	N/A	**0**	**1**	**0**	**1**	**0**
	0 – 25.0 V	0 – 20.0 V	N/A	**0**	**1**	**0**	**0**	**1**
	0 – 12.5 V	0 – 10.0 V	0 – 10.0 V	**0**	**0**	**0**	**0**	**0**
	0 – 6.25 V	0 – 5.00 V	0 – 5.00 V	**0**	**0**	**0**	**0**	**1**
	0 – 3.125V	0 – 2.50 V	0 – 2.50 V	**0**	**0**	**0**	**1**	**0**
	0 – 1.5625 V	0 – 1.25 V	0 – 1.25 V	**0**	**0**	**0**	**1**	**1**
	0 – .78125 V	0- 0.625 V	0- 0.625 V	**0**	**0**	**1**	**0**	**0**
Bipolar RANGE	±50.0 V	±40.0 V	±40.0 V	**1**	**1**	**0**	**1**	**0**
	±25.0 V	±20.0 V	±20.0 V	**1**	**1**	**0**	**0**	**1**
	±12.5 V	±10.0 V	±10.0 V	**1**	**0**	**0**	**0**	**0**
	±6.25 V	±5.00 V	±5.00 V	**1**	**0**	**0**	**0**	**1**
	±3.125V	±2.50 V	±2.50 V	**1**	**0**	**0**	**1**	**0**
	±1.5625 V	±1.25 V	±1.25 V	**1**	**0**	**0**	**1**	**1**
	±0.78125 V	±0.625 V	±0.625 V	**1**	**0**	**1**	**0**	**0**

A/D Filter Break Frequency

The break frequency is the 3 db point of a single pole low pass filter. Enter desired frequency for each channel between 10 Hz to 10 kHzas a 16 bit binary number. Zero disables filter.

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII “1” in upper byte and ASCII space in lower byte for Module Design Version “1 ” is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN VERSION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII “1”								**ASCII “ ”**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII “B” in upper byte and ASCII space in lower byte for Module Design Revision “B ” is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII “B”								**ASCII “ ”**								

Module DSP

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4331h

Read register to determine Module ID in ASCII. For example, find ASCII “C” in upper byte and ASCII “1” in lower byte, for Module “C1,” together 4331h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “C”								ASCII “1”								

BIT Status

Check the corresponding bit for a channel’s BIT Status. A “0” =Normal; “1” = Non-compliant A/D conversion (outside 0.2% FS accuracy spec). Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status

Check for an open or disconnect to the A/D input. Status of each channel is indicated at its corresponding bit. A “0” =Normal and “1” = Open. An open or disconnect to the input of an A/D channel is detected within 10 seconds and will latch the corresponding bit in the *Open Status* register. Reading any status bit will unlatch the entire register. Open Status is part of background testing and the status register may be checked or polled at any given time. NOTE: Does not apply to Current Measurement Module C3.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status	X	X	X	X	X	X	Ch. 10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status Interrupt Enable

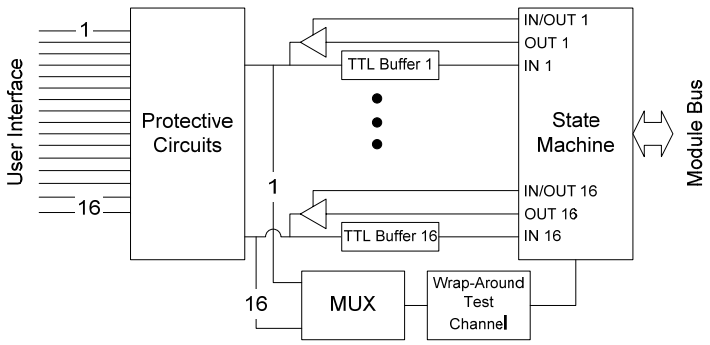
Set the bit to enable interrupts for the corresponding channel monitored for Open Status. Open Status does NOT apply to high voltage (20V to 80V) or current measurement modules.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

I/O DIGITAL TTL, (MODULE D1)

Digital (TTL) I/O channels (in banks of 16) are programmable for either Input or Output and include extensive diagnostics. Interrupt can be selected, for each channel, to indicate transition on rising edge, transition on falling edge, or both. De-bounce circuits for each channel offer a selectable time delay to eliminate false signals resulting from contact bounce commonly experienced with mechanical relays and switches. Each TTL channel has an internal 110KΩ pull-down resistor. All inputs are continually scanned and the data is double buffered for immediate availability.

TTL Module Block Diagram



The (D2) test initiates **automatic** background BIT testing which tests and validates channel processing (data read or write logic), tests for circuit over-current conditions and provides status for threshold signal transitioning. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus.

MODULE MEMORY MAP

000	Write Output,	Ch.1-16 R/W	0E0	Debounce time	Ch.11	R/W	194	Module DSP[1]		R
004	Read I/O,	Ch.1-16 R/W	0F4	Debounce time	Ch.12	R/W	198	Module FPGA[1]		R
018	Debounce time	Ch.1 R/W	108	Debounce time	Ch.13	R/W	19C	Module ID		R
02C	Debounce time	Ch.2 R/W	11C	Debounce time	Ch.14	R/W	1A0	Status Fault	Ch.01-16	R
040	Debounce time	Ch.3 R/W	130	Debounce time	Ch.15	R/W	1A8	Status Over-Current	Ch.01-16	R
054	Debounce time	Ch.4 R/W	144	Debounce time	Ch.16	R/W	1B8	Status Lo-Hi Transition	Ch.01-16	R
068	Debounce time	Ch.5 R/W	148	Input/Output Format	Ch.01-8	R/W	1BC	Status Hi-Lo Transition	Ch.01-16	R
07C	Debounce time	Ch.6 R/W	14C	Input/Output Format	Ch.09-16	R/W	000	Interrupt Fault Enable	Ch.01-16	R/W
090	Debounce time	Ch.7 R/W	178	Reset Over-Current	Ch.1-16	R/W	1D8	Interrupt Over-Current Enable	Ch.01-16	R/W
0A4	Debounce time	Ch.8 R/W	18C	Module Design Version[1]		R	1E8	Interrupt Lo-Hi Transition Enable	Ch.01-16	R/W
0B8	Debounce time	Ch.9 R/W	190	Module Design Revision[1]		R	1EC	Interrupt Hi-Lo Transition Enable	Ch.01-16	R/W
0CC	Debounce time	Ch.10 R/W								

Note: 1. Pending

Write Output

When a channel is configured for Output, write logic level High (“1”) or Low (“0”) to associated channel bit, in 16 bit binary word. Each bit corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Read I/O

Independent of channel configuration (Input or Output), read logic state High (“1”) or Low (“0”) as defined by channel threshold values. Each bit of 16-bit binary word corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

De-bounce time

Enter required de-bounce time into appropriate channel registers. Enter time in 1.28μs increments, up to 326.40 μsec. LSB= 1.28 μs. Value is 8 bits (MSBs=don't care). Once a signal level is a logic voltage level period longer than the De-bounce time (Logic High > 2.0 v, and Logic Low < 0.6 v), a logic transition is validated. Signal pulse widths less than De-bounce time are filtered or ignored. Once valid, the interrupt transition register channel flag is set and the output logic changes state. Enter a value of 0 to disable De-bounce filtering. De-bounce defaults to 00h upon reset.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
									163.84	81.92	40.96	20.48	10.24	5.12	2.56	1.28	value in mSec (LSB=1.28μS)
DE-BOUNCE TIME	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input/Output Format

Configure channels in groups of 8. Write integer 0 for input, 3 for output: Default is configured for Input.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INPUT/OUTPUT CH 01-08	Ch.08		Ch.07		Ch.06		Ch.05		Ch.04		Ch.03		Ch.02		Ch.01		Channel
INPUT/OUTPUT CH 09-16	Ch.16		Ch.15		Ch.14		Ch.13		Ch.12		Ch.11		Ch.10		Ch.09		Channel
INPUT/OUTPUT	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT

Integer	D_H	D_L	
0	**0**	**0**	Input
3	**1**	**1**	Output

Reset Over-Current

Write integer "1" to reset all sixteen channels (per module). Used to reset disabled channel(s) following an over-current condition. When reset process is complete, processor will write a "0" back to the *Reset Over-Current* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESET OVER-CURRENT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	D=DATA BIT

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN VERSION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP

Type: binary word
Range: 0 to 65535

Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4431h

Read register to determine Module ID in ASCII. For example, find ASCII “D” in upper byte and ASCII “1” in lower byte for Module “D1,” together 4431h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “D”								ASCII “1”								

Automatic background BIT testing

BIT is always enabled and continually checks that each channel is functional. This capability is accomplished by an additional test comparator that is incorporated into each 16 channel module. The test comparator is sequentially connected across each channel and is compared against the operational channel. Depending upon configuration, the Input data read or Output logic write of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. Low to High and High to Low logic transitions are indicated. Additional testing of output logic indicates Over-current condition when output logic is invalid for a period greater than 80µs.

Status indications

Fault – processing (data read or write logic) is inconsistent with redundant test circuit.
Status is indicated within 15 seconds. A fault is latched until read. (Testing takes approx. 1 second per channel)

Lo-Hi Transition – If a Lo to High transition is sensed, status is indicated (bit is set) within 40µs.
Hi-Low Transition – If a High to Low transition is sensed, status is indicated (bit is set) within 40µs.

Over-current – If over-current or overload condition is sensed, status is indicated (bit is set) within 80µs.
Output is however, immediately disabled at time of over-current condition.

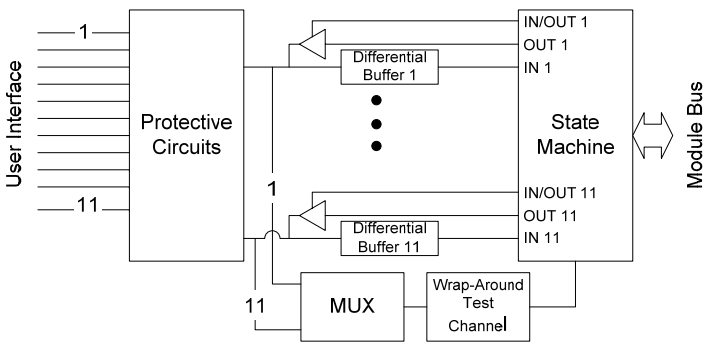
When status is “indicated,” or bit is “set,” bit value is logic “1.” Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

I/O DIGITAL DIFFERENTIAL MULTI-MODE TRANSCEIVERS (MODULE D2)

Differential RS422/RS485 I/O channels (in banks of 11) are programmable for either Input or Output and include extensive diagnostics. Each Differential input channel has a selectable internal resistor (120Ω or >12kΩ) across its inputs. Interrupt can be selected, for each channel, to indicate transition on rising edge, transition on falling edge, or both. De-bounce circuits for each channel offer a selectable time delay to eliminate false signals resulting from contact bounce commonly experienced with mechanical relays and switches. All inputs are continually scanned and the data is double buffered for immediate availability.

Differential Module Block Diagram



The (D2) test initiates **automatic** background BIT testing which tests and validates channel processing (data read or write logic), tests for circuit over-current conditions and fault status. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus.

MODULE MEMORY MAP

000	Write Output,	Ch.1-11	R/W	0B8	Debounce time	Ch.9	R/W	19C	Module ID	R
004	Read I/O,	Ch.1-11	R/W	0CC	Debounce time	Ch.10	R/W	1A0	Status Fault	Ch.01-11	R
018	Debounce time	Ch.1	R/W	0E0	Debounce time	Ch.11	R/W	1A8	Status Over-Current	Ch.01-11	R
02C	Debounce time	Ch.2	R/W	144	Input Termination	Ch 01-11	R/W	1B8	Status Lo-Hi Transition	Ch.01-11	R
040	Debounce time	Ch.3	R/W	148	Input/Output Format	Ch.1-8	R/W	1BC	Status Hi-Lo Transition	Ch.01-11	R
054	Debounce time	Ch.4	R/W	14C	Input/Output Format	Ch.9-11	R/W	000	Interrupt Fault Enable	Ch.01-11	R/W
068	Debounce time	Ch.5	R/W	18C	Module Design Version[1]		R	1D8	Interrupt Over-Current Enable	Ch.01-11	R/W
07C	Debounce time	Ch.6	R/W	190	Module Design Revision[1]		R	1E8	Interrupt Lo-Hi Transition Enable	Ch.01-11	R/W
090	Debounce time	Ch.7	R/W	194	Module DSP[1]		R	1EC	Interrupt Hi-Lo Transition Enable	Ch.01-11	R/W
0A4	Debounce time	Ch.8	R/W	198	Module FPGA[1]		R				

Note: 1. Pending

Write Output

When a channel is configured for Output, write logic level High (“1”) or Low (“0”) to associated channel bit, in 16 bit binary word. Each bit corresponds to one of 11 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
						11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Read I/O

Independent of channel configuration (Input or Output), read logic state High (“1”) or Low (“0”). Each bit of 16-bit binary word corresponds to one of 11 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
						11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

De-bounce time

Enter required de-bounce time into appropriate channel registers. Enter time in 1.28μs increments, up to 326.40 μsec. LSB= 1.28 μs. Value is 8 bits (MSBs=don't care). Once a signal level is a logic voltage level period longer than the De-bounce time (Logic High > 2.0 v, and Logic Low < 0.6 v), a logic transition is validated. Signal pulse widths less than De-bounce time are filtered or ignored. Once valid, the interrupt transition register channel flag is set and the output logic changes state. Enter a value of 0 to disable De-bounce filtering. De-bounce defaults to 00h upon reset.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
									163.84	81.92	40.96	20.48	10.24	5.12	2.56	1.28	value in mSec (LSB=1.28μS)
DE-BOUNCE TIME	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input Termination Control

Each differential input pair can be programmed to have an input termination of 120 Ω or >12k Ω. Write logic'1' to select 120 Ω for each individual channel. Default is >12k Ω.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
						11	10	9	8	7	6	5	4	3	2	1	Channel
INPUT TERMINATION	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input/Output Format

Write integer 0 for input, 3 for output: Default is configured for Input.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INPUT/OUTPUT CH 01-08	Ch.08		Ch.07		Ch.06		Ch.05		Ch.04		Ch.03		Ch.02		Ch.01		Channel
INPUT/OUTPUT CH 09-11											Ch.11		Ch.10		Ch.09		Channel
INPUT/OUTPUT	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT

Integer	D_H	D_L	
0	**0**	**0**	Input
3	**1**	**1**	Output

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP

Type: binary word
Range: 0 to 65535

Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4332h

Read register to determine Module ID in ASCII. For example, find ASCII “D” in upper byte and ASCII “2” in lower byte for Module “D2,” together 4432h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “D”								ASCII “2”								

Automatic background BIT testing

BIT is always enabled and continually checks that each channel is functional. This capability is accomplished by an additional test comparator that is incorporated into each 11 channel module. The test comparator is sequentially connected across each channel and is compared against the operational channel. Depending upon configuration, the Input data read or Output logic write of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. Low to High and High to Low logic transitions are indicated. Additional testing of output logic indicates Over-current condition when output logic is invalid for a period greater than 80µs.

Status indications

Fault – processing (data read or write logic) is inconsistent with redundant test circuit.
Status is indicated within 15 seconds. A fault is latched until read. (Testing takes approx. 1 second per channel)

Lo-Hi Transition – If a Lo to High transition is sensed, status is indicated within 40µs.
Hi-Low Transition – If a High to Low transition is sensed, status is indicated within 40µs.

Over-current – If over-current or overload condition is sensed, status is indicated (bit is set) within 80µs. Output is however, immediately disabled at time of over-current condition. Over-current is re-checked every 6ms. If applicable output is re-enabled and channel is reset.

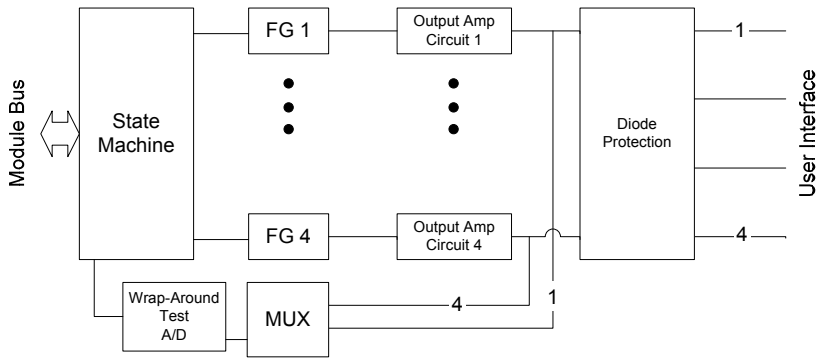
A ”0” indicates Passing and “1” Failing status. Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

SIGNAL GENERATOR (MODULE E)

Signal Generator modules generate one of a selection of waveforms, sine, triangular, or square wave, per channel, programmable in frequency and amplitude. Use of an individual A/D self test channel, on a rotating basis, verifies that the channel is operating properly in frequency, amplitude, and DC offset. See wrap-around test registers for BIT data

Signal Module Block Diagram



Operating at all times is a background Built-In-Test (BIT), where each channel is checked to a test accuracy of 2% FS. Any failure triggers an Interrupt (if enabled) with the results available in status registers. BIT is intended for use with steady state signals; any change in channel configuration (amplitude, frequency, etc) requires up to 12 seconds before wrap data reflects that change. Multiple changes in channel configuration in less than 12 seconds may trigger false BIT failures. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card.

MODULE MEMORY MAP

000	Ch.1 Frequency High	R/W	040	Ch.3 DC Offset	R/W	0A0	Ch.3 Wrap-around Frequency High	R
004	Ch.1 Frequency Low	R/W	044	Ch.3 Mode	R/W	0A4	Ch.3 Wrap-around Frequency Low	R
008	Not used		048	Ch.4 Freq Hi	R/W	0A8	Ch.3 Wrap-around Amplitude	R
00C	Ch.1 Amplitude	R/W	04C	Ch.4 Freq Lo	R/W	0AC	Ch.3 Wrap-around DC Offset	R
010	Ch.1 DC Offset	R/W	050	Ch.4 Phase	R/W	0B0	Ch.4 Wrap-around Frequency High	R
014	Ch.1 Mode	R/W	054	Ch.4 Amplitude	R/W	0B4	Ch.4 Wrap-around Frequency Low	R
018	Ch.2 Freq Hi	R/W	058	Ch.4 DC Offset	R/W	0B8	Ch.4 Wrap-around Amplitude	R
01C	Ch.2 Freq Lo	R/W	05C	Ch.4 Mode	R/W	0BC	Ch.4 Wrap-around DC Offset	R
020	Ch.2 Phase	R/W	080	Ch.1 Wrap-around Frequency High	R	18C	Module Design Version[1]	
024	Ch.2 Amplitude	R/W	084	Ch.1 Wrap-around Frequency Low	R	190	Module Design Revision[1]	R
028	Ch.2 DC Offset	R/W	088	Ch.1 Wrap-around Amplitude	R	194	Module DSP[1]	R
02C	Ch.2 Mode	R/W	08C	Ch.1 Wrap-around DC Offset	R	198	Module FPGA[1]	R
030	Ch.3 Freq Hi	R/W	090	Ch.2 Wrap-around Frequency High	R	19C	Module ID	R
034	Ch.3 Freq Lo	R/W	094	Ch.2 Wrap-around Frequency Low	R	1A0	BIT Status Ch.1-4	R
038	Ch.3 Phase	R/W	098	Ch.2 Wrap-around Amplitude	R	1C0	BIT Stat Interrupt Enable Ch.1-4	R/W
03C	Ch.3 Amplitude	R/W	09C	Ch.2 Wrap-around DC Offset	R			

Note: 1. Pending

Frequency

Type: 32 bit unsigned integer
Range: 0 – 130,000 (from 1 to 9 Hz, amplitude is functional, but not to accuracy specification)
Read/Write: R/W
Initialized Value: 1000

Frequency High and *Frequency Low* registers combined to determine desired frequency in 1 Hz resolution. LSB is 1 Hz. Frequency is updated on write to Low register. Out-of-range data will be changed to the maximum allowable value. When phase locked, phase is reset when channel 1frequency is changed. If phase is NOT locked, phase remains unchanged when frequency is changed.

FREQUENCY HIGH REGISTER																FREQUENCY LOW REGISTER															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Phase

Type: 16-bit signed integer
Range: ±180 degrees
Read/Write: R/W
Initialized Value: 0

Enter the desired phase offset, relative to channel 1. LSB is approximately 0.088°. When phase locked, phase is reset when channel 1frequency is changed. If phase is NOT locked, phase remains unchanged when frequency is changed. Enter as per formula,

Phase = Register Value / 32768 x 180 Degrees.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PHASE	S	D	D	D	D	D	D	D	D	D	D	D	X	X	X	X	S=SIGN BIT, D=DATA BIT

Amplitude

Type: 16 bit unsigned integer
Range: 0 to 65535 (0 to 10 volts peak E1 ; 0 to 15 volts peak E2)
Read/Write: R/W
Initialized Value: 0

Value determines peak amplitude of selected waveform. Amplitude in combination with the programmed DC Offset cannot be greater that the maximum or full scale output of that module. For module E1, resolution is 10/65536 or approximately 0.15 millivolts. For module E2 resolution is 15/65536 or approximately 0.22 millivolts. From 1 to 9 Hz, amplitude is not accurate. Enter as per formula,

Peak-to-Peak Voltage = 10*Value/65535 Volts Peak, for module E1, (≤ 10 – magnitude of DC Offet).

Peak-to-Peak Voltage = 15*Value/65535 Volts Peak, for module E2, (≤ 15 – magnitude of DC Offet).

Where Volts Peak is half Peak-to-Peak Voltage. Out-of-range data will be changed to the maximum allowable value. From 1 to 9 Hz, amplitude is functional, but not to accuracy specification.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

DC Offset

Type: 16 bit signed integer
Range: -32767 to +32767 (±10 volts E1 ; ±15 volts E2)
Read/Write: R/W
Initialized Value: 0

Value determines DC offset of selected waveform, in 0.30 millivolt resolution.
Enter as per formula,

DC Offset Voltage = 10*Value/32768 Volts DC, for Module E1

DC Offset Voltage = 15*Value/32768 Volts DC, for Module E2

Out-of-range data will be changed to the maximum allowable value.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Mode

Type: binary word
Range: 0, 1, or 2
Read/Write: R/W
Initialized Value: 0 (Sine Wave)

This register is used to select desired waveform using bits D0 and D1. Use bit D2 to enable phase lock function. L=1 to enable, L=0 to disable. When phase lock is enabled, channel 2, 3, and 4 are phase locked to the master signal channel 1. When phased locked, the signal of channels 2, 3 and 4 will be identical to channel 1 in *frequency* and *type* (sine, triangular or square). When phase locked, phase is reset when frequency is changed.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODE and LOCK	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**0**	**0**	SINE WAVE
	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**0**	**1**	TRIANGULAR WAVE
	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**1**	**0**	SQUARE WAVE
	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**1**	**1**	SINE WAVE (same as 00)

Wrap-around Frequency

Type: 32 bit unsigned integer
Range: 0 – 130,000 (from 1 to 9 Hz, amplitude is functional, but not to accuracy specification)
Read/Write: R
Initialized Value: N/A

Read *Wrap-around Frequency High* and *Frequency Low* registers combined to determine desired frequency in 1 Hz resolution. LSB is 1 Hz.

FREQUENCY HIGH REGISTER																	FREQUENCY LOW REGISTER															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

Wrap-around Amplitude

Type: 16 bit unsigned integer
Range: 0 to 65535 (0 to 10 volts peak E1 ; 0 to 15 volts peak E2)
Read/Write: R
Initialized Value: N/A

Read *Wrap-around Amplitude* for D2 BIT test value to verify peak amplitude of selected waveform. For module E1, resolution is 10/65536 or approximately 0.15 millivolts. For module E2 resolution is 15/65536 or approximately 0.22 millivolts. From 1 to 9 Hz, amplitude is not accurate. Decode value as per formula,

Peak-to-Peak Voltage = 10*Value/65535 Volts Peak, for module E1

Peak-to-Peak Voltage = 15*Value/65535 Volts Peak, for module E2

where Volts Peak is half Peak-to-Peak Voltage.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Wrap-around DC Offset

Type: 16 bit signed integer
Range: -32767 to +32767 (±10 volts E1 ; ±15 volts E2)
Read/Write: R
Initialized Value: N/A

Read *Wrap-around DC Offset* for D2 BIT test value to verify DC offset of selected waveform, in 0.30 millivolt resolution. Decode value as per formula,

DC Offset Voltage = 10*Value/32768 Volts DC, for Module E1

DC Offset Voltage = 15*Value/32768 Volts DC, for Module E2

Out-of-range data will be changed to the maximum allowable value.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN VERSION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1"								ASCII " "								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "B"								ASCII " "								

Module DSP

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4531h

Read register to determine Module ID in ASCII. For example, find ASCII "E" in upper byte and ASCII "1" in lower byte, for Module "E1," together 4531h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "E"								ASCII "1"								

BIT Status

Type: binary word
Range: 0 to 15
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Built-In-Test (BIT) Status. Channel Status Data bit (Chn, where n is 1, 2, 3 or 4) is fail, high true, and indicates that the channel is not operating spec compliant. Passing BIT status indicates that channel Frequency, Amplitude and DC Offset is as programmed. Status is latched. Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time. BIT is operating at all times and cannot be enabled or disabled using the General use *Test Enable* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	CHANNEL STATUS BIT

BIT Status Interrupt Enable

Type: binary word
Range: 0 to 15
Read/Write: R/W
Initialized Value: 0

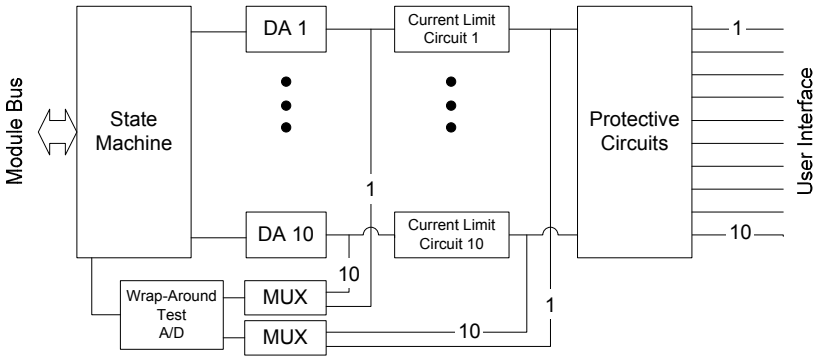
Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 0 to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS INTR ENA	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	INTERRUPT ENABLE

D/A (MODULE F OR J)

Ten (10) D/A channels are provided per module and includes extensive diagnostics. Overloaded outputs will be detected, with the results displayed in a status word. This module incorporates major diagnostic capabilities that offer substantial improvements to system reliability because user is alerted to malfunctions within 5 seconds. Two different tests, one off-line (D2) and one on-line (D3) can be selected:

DA Module Block Diagram



The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 0.2% FS and monitored for shorted output. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

The (D3) test uses an internal A/D that measures all D/A channels while they remain connected to the I/O. Each channel will be checked to a test accuracy of 0.2% FS. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from "1" to "0". The test can be stopped at any time. This test requires no user programming and can be enabled or disabled via the bus. **CAUTION:** D/A Outputs are active during this test. Check connected loads for interaction.

D/A Over Current (short circuit) monitoring is disabled during D3 testing.

MODULE MEMORY MAP

000	Data 1	R/W	028	Polarity 1	R/W	050	Wrap-around 1	R/W	18C	Module Design Version[1]	R
004	Data 2	R/W	02C	Polarity 2	R/W	054	Wrap-around 2	R/W	190	Module Design Revision[1]	R
008	Data 3	R/W	030	Polarity 3	R/W	058	Wrap-around 3	R/W	194	Module DSP[1]	R
00C	Data 4	R/W	034	Polarity 4	R/W	05C	Wrap-around 4	R/W	198	Module FPGA[1]	R
010	Data 5	R/W	038	Polarity 5	R/W	060	Wrap-around 5	R/W	19C	Module ID	R
014	Data 6	R/W	03C	Polarity 6	R/W	064	Wrap-around 6	R/W	1A0	BIT Status Ch.1-10	R
018	Data 7	R/W	040	Polarity 7	R/W	068	Wrap-around 7	R/W	1A8	Over Current Status Ch.1-10	R
01C	Data 8	R/W	044	Polarity 8	R/W	06C	Wrap-around 8	R/W	1C0	BIT Stat Interrupt Enable Ch.1-10	R/W
020	Data 9	R/W	048	Polarity 9	R/W	070	Wrap-around 9	R/W	1D8	Over Current Interrupt Enable Ch.1-10	R/W
024	Data 10	R./W	04C	Polarity 10	R/W	074	Wrap-around 10	R/W			

Note: 1. Pending

Write D/A output

If using bi-polar mode, write 16 bit 2's complement word to the channel's *Data register* (7FFFh=+FS, 8000h=-FS) If using unipolar mode, write 16 bit binary word to the channel's *Data register* (range: 0 to FFFFh=FS).

D/A Output Polarity

Write integer 4 to the channel's *D/A Polarity register* for unipolar mode. Write integer 0 to the channel's *D/A range register* for bi-polar mode.

D/A Wrap-Around

Read D/A *wrap-around data* register, 16 bit 2's complement word (7FFFh=+FS, 8000h=-FS) bipolar mode, or 16 bit binary word (range 0 to FFFFh=FS)

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1"								ASCII " "								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "B"								ASCII " "								

Module DSP

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4E37h

Read register to determine Module ID in ASCII. For example, find ASCII "J" in upper byte and ASCII "7" in lower byte for Module "J7," together 4E37h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "J"								ASCII "7"								

BIT Status

Check the corresponding bit for a channel's BIT Status. A "0" =Normal; "1" = Non-compliant D/A conversion (outside 0.2% FS accuracy spec). Reading any status bit will cause that bit to be unlatched. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status

Check the corresponding bit of the *Over Current Status* registers for over current draw for each active channel. A "0" =Normal; "1" = Over Current. An over current draw from the output of any D/A channel is detected within 2 seconds and will latch the corresponding bit in the *Over Current Status* register. Reading any status bit will cause unlatch the entire register. Over Current Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status	X	X	X	X	X	X	Ch. 10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status Interrupt Enable

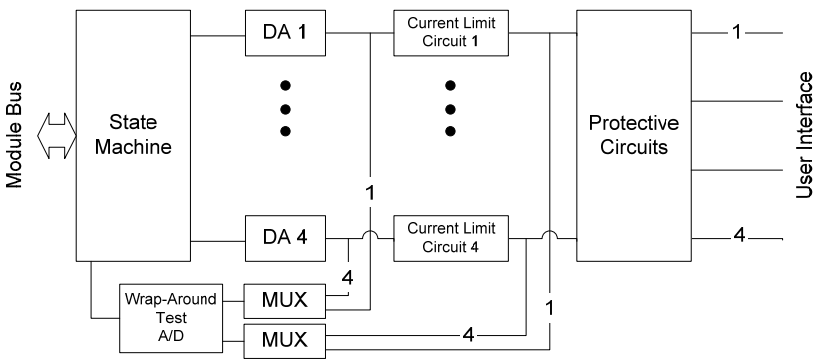
Set the bit to enable interrupts for the corresponding channel monitored for Over Current Status.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status Intr Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

HIGH VOLTAGE D/A (MODULE J7)

Four (4) D/A channels are provided per module and includes extensive diagnostics. To save power, DC-to-DC output drive is internally scaled according to programmed output range. Overloaded outputs will be detected, with the results displayed in a status word. This module incorporates major diagnostic capabilities that offer substantial improvements to system reliability because user is alerted to malfunctions within 5 seconds. Two different tests, one off-line (D2) and one on-line (D3) can be selected:

High Voltage DA Module Block Diagram



The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 2% FS and monitored for shorted output. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

The (D3) test uses an internal A/D that measures all D/A channels while they remain connected to the I/O. Each channel will be checked to a test accuracy of 2% FS. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from "1" to "0". The test can be stopped at any time. This test requires no user programming and can be enabled or disabled via the bus. **CAUTION:** D/A Outputs are active during this test. Check connected loads for interaction.

D/A Over Current (short circuit) monitoring is disabled during D3 testing.

MODULE MEMORY MAP

000	Data 1	R/W	020	Polarity 3	R/W	194	Module DSP[1]	R
004	Data 2	R/W	024	Polarity 4	R/W	198	Module FGPA[1]	R
008	Data 3	R/W	028	Wrap-around 1	R/W	19C	Module ID	R
00C	Data 4	R/W	02C	Wrap-around 2	R/W	1A0	BIT Status Ch.1-4	R
010	Range 1 & 2	R/W	030	Wrap-around 3	R/W	1A8	Over Current Status Ch.1-4	R
014	Range 3 & 4	R/W	034	Wrap-around 4	R/W	1C0	BIT Stat Interrupt Enable Ch.1-4	R/W
018	Polarity 1	R/W	18C	Module Design Version[1]	R	1D8	Over Current Interrupt Enable Ch.1-4	R/W
01C	Polarity 2	R/W	190	Module Design Revision[1]	R			

Note: 1. Pending

Write D/A Output

If using bi-polar mode, write 16 bit 2's complement word to the channel's *Data register* (7FFFh=+FS, 8000h=-FS) If using unipolar mode, write 16 bit binary word to the channel's *Data register* (range: 0 to FFFFh=FS). Because output resolution is 12bits, enter LSBs D0 through D3 as zero. At power-on, output is initialized to 0 volts.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	0	0	0	0	D=DATA BIT

D/A Output Range

Program voltage range for channel pairs (1 & 2, or 3 & 4) from 20 to 80 volts. For 20 volts, enter integer 20. Resolution is 10 volts. 10 ma/channel maximum (source or sink) for up to 80VDC.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
										64	32	16	8	4	2	1	value in volts (LSB=1volt)
RANGE	X	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D=DATA BIT
												1	0	1	0	0	20 volts
												1	1	1	1	0	30 volts
											1	0	1	0	0	0	40 volts
											1	1	0	0	1	0	50 volts
											1	1	1	1	0	0	60 volts
										1	0	0	0	1	1	0	70 volts
										1	0	1	0	0	0	0	80 volts

D/A Output Polarity

Write integer 4 to the channel's *D/A Polarity register* for unipolar mode. Write integer 0 to the channel's *D/A Polarity register* for bi-polar mode.

D/A Wrap-Around

Read D/A *wrap-around data* register, 16 bit 2's complement word (7FFFh=+FS, 8000h=-FS) bipolar mode, or 16 bit binary word (range 0 to FFFFh=FS)

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1"								ASCII " "								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "B"								ASCII " "								

Module DSP

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4A37h

Read register to determine Module ID in ASCII. For example, find ASCII "J" in upper byte and ASCII "1" in lower byte for Module "J7," together 4A37h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "J"								ASCII "7"								

BIT Status

Check the corresponding bit for a channel's BIT Status. A "0" =Normal; "1" = Non-compliant D/A conversion (outside 2% FS accuracy spec). Reading any status bit will cause that bit to be unlatched. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status

Check the corresponding bit of the *Over Current Status* registers for over current draw for each active channel. A "0" =Normal; "1" = Over Current. An over current draw from the output of any D/A channel is detected within 2 seconds and will latch the corresponding bit in the *Over Current Status* register. Reading any status bit will cause unlatch the entire register. Over Current Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

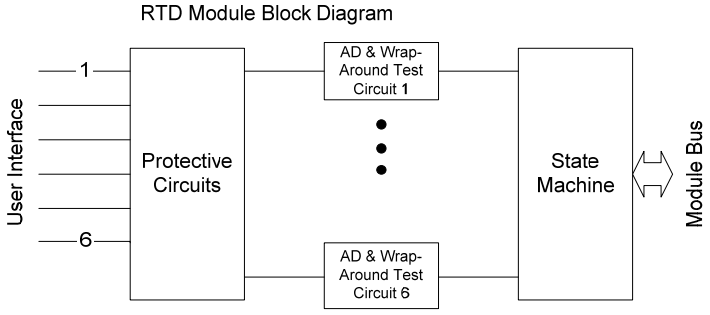
Over Current Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored for Over Current Status.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status Intr Enable	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

RTD (MODULE G)

The RTD channels use individual A/D converters. All RTD channels are self-calibrating because each channel, on a rotating basis, is automatically calibrated to eliminate offset and gain errors. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution. Open inputs will be detected, with the results displayed in a status word. All inputs are double buffered for immediate availability. External excitation not required.



The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 0.2% FS and monitored for open input. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus.

RTD Open Circuit monitoring is disabled during D3 testing.

MODULE MEMORY MAP

000	Resistance 1	R	01C	Range 2	R/W	038	3 or 4 Wire Mode 3	R/W	198	Module FPGA[2]	R
004	Resistance 2	R	020	Range 3	R/W	03C	3 or 4 Wire Mode 4	R/W	19C	Module ID	R
008	Resistance 3	R	024	Range 4	R/W	040	3 or 4 Wire Mode 5	R/W	1A0	BIT Status Ch.1-6	R
00C	Resistance 4	R	028	Range 5	R/W	044	3 or 4 Wire Mode 6	R/W	1A4	Open Status Ch.1-6	R
010	Resistance 5	R	02C	Range 6	R/W	18C	Module Design Version[2]	R	1C0	BIT Stat Interrupt Enable Ch.1-6	R/W
014	Resistance 6	R	030	3 or 4 Wire Mode 1[1]	R/W	190	Module Design Revision[2]	R	1D4	Open Stat INTR Enable Ch.1-6	R/W
018	Range 1	R/W	034	3 or 4 Wire Mode 2[1]	R/W	194	Module DSP[2]	R			

Note: 1. For 3 or 4 Wire Modes, Consult Factory
2. Pending

Resistance

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Resistance measurement is a binary word and is dependant upon range.
For example, if the 0.01 ohms per count range is selected: 2710h x 0.01 = 10000 x 0.01 = 100 ohms.

The resistance/temperature relationship varies among RTDs and is function of its composite material (ex, Platinum, Copper, Nickel-Iron, Nickel, etc). An RTD's "Alpha" Temperature Coefficient and its nominal resistance (at say 0°C), while operating within its applicable resistance range, provide for a first order approximation.

For best accuracy, use resistance/temperature relationship provided by the RTD manufacture:

Select associated *Range* (0-655, or 1-2000)
Read *Resistance* and scale accordingly (0.01 Ω / bit , or 0.03 Ω / bit.)

Calculate temperature using RTD manufacture provided resistance/temperature relationship (a quadratic equation).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESISTANCE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Range

Type: 16 bit unsigned integer
Range: 0 or 1
Read/Write: R/W
Initialized Value: 0

Write “0” for a 0-655 ohm output range, 0.01 Ω / bit.
Write “1” for a 1-2000 ohm output range, 0.03 Ω / bit.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RANGE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

3 or 4 Wire Mode

Consult Factory.

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII “1” in upper byte and ASCII space in lower byte for Module Design Version “1 ” is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “1”								ASCII “ ”								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII “B” in upper byte and ASCII space in lower byte for Module Design Revision “B ” is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “B”								ASCII “ ”								

Module DSP

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Read register to determine Module ID in ASCII. For example, find ASCII “G” in upper byte and ASCII “1” in lower byte for Module “G1,” together 4731h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “G”								ASCII “1”								

BIT Status

Check the corresponding bit for a channel’s BIT Status. A “0” =Normal; “1” = Non-compliant A/D conversion (outside 0.2% FS accuracy spec). Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status

Check the corresponding bit of the *Open Status* registers for open/disconnected RTD for each active channel. A “0” =Normal; “1” = Open (detected after 2 seconds). Reading any status bit will cause that bit to be unlatched. Open Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status	X	X	X	X	X	X	Ch. 10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status Interrupt Enable

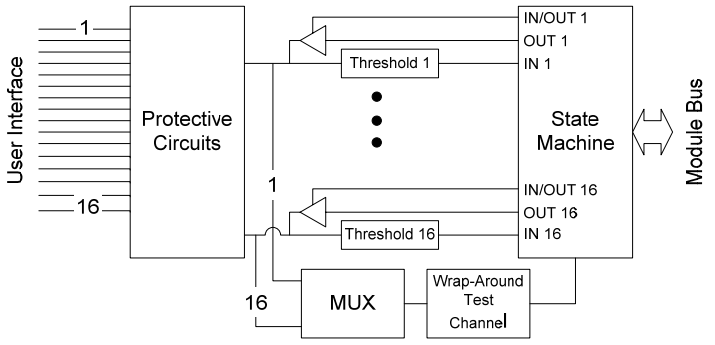
Set the bit to enable interrupts for the corresponding channel monitored for Open Status.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

I/O DISCRETE (MODULE K)

Discrete (LSI) channels are programmable for either Input or Output. When programmed for Input, they can be used for either voltage or contact sensing. Channels set for contact sensing can be programmed for either pull-up or pull-down. Our unique design eliminates the need for pull-up resistors or mechanical jumpers. Instead, we offer a current source (in groups of 4) that user programs to a desired current level. When programmed for Output, each channel can be set for either High-side, Lo-side or Push-Pull operation. Modules K2 and K4 add diode clamping (useful for inductive loads, such as relays) and thermal protection. Module K2 is signal isolated from the cPCI bus while both module K2 and K4 are power isolated from the cPCI bus. There are 4 user provided Vcc inputs for each 16 channel module. There is one Vcc input for each four channel bank. Vcc must be wired for proper operation.

Discrete IO Module Block Diagram



Module Memory Map

000	Write Output	Ch.01-16	R/W	098	Upper Threshold	Ch.08	R/W	130	De-bounce time	Ch.15	R/W
004	Read I/O	Ch.01-16	R	09C	Lower Threshold	Ch.08	R/W	134	Max High Threshold	Ch.16	R/W
008	Max High Threshold	Ch.01	R/W	0A0	Min Low Threshold	Ch.08	R/W	138	Upper Threshold	Ch.16	R/W
00C	Upper Threshold	Ch.01	R/W	0A4	De-bounce time	Ch.08	R/W	13C	Lower Threshold	Ch.16	R/W
010	Lower Threshold	Ch.01	R/W	0A8	Max High Threshold	Ch.09	R/W	140	Min Low Threshold	Ch.16	R/W
014	Min Low Threshold	Ch.01	R/W	0AC	Upper Threshold	Ch.09	R/W	144	De-bounce time	Ch.16	R/W
018	De-bounce time	Ch.01	R/W	0B0	Lower Threshold	Ch.09	R/W	148	Input/Output Format	Ch.01-08	R/W
01C	Max High Threshold	Ch.02	R/W	0B4	Min Low Threshold	Ch.09	R/W	14C	Input/Output Format	Ch.09-16	R/W
020	Upper Threshold	Ch.02	R/W	0B8	De-bounce time	Ch.09	R/W	150	Current For Sink/Source, Bank 1	Ch.01-04	R/W
024	Lower Threshold	Ch.02	R/W	0BC	Max High Threshold	Ch.10	R/W	154	Current For Sink/Source, Bank 2	Ch.05-08	R/W
028	Min Low Threshold	Ch.02	R/W	0C0	Upper Threshold	Ch.10	R/W	158	Current For Sink/Source, Bank 3	Ch.09-12	R/W
02C	De-bounce time	Ch.02	R/W	0C4	Lower Threshold	Ch.10	R/W	15C	Current For Sink/Source, Bank 4	Ch.13-16	R/W
030	Max High Threshold	Ch.03	R/W	0C8	Min Low Threshold	Ch.10	R/W	160	Pull Up/Down Current Config	Ch.01-16	R/W
034	Upper Threshold	Ch.03	R/W	0CC	De-bounce time	Ch.10	R/W	168	Vcc Value, Bank 1	Ch.01-04	R
038	Lower Threshold	Ch.03	R/W	0D0	Max High Threshold	Ch.11	R/W	16C	Vcc Value, Bank 2	Ch.05-08	R
03C	Min Low Threshold	Ch.03	R/W	0D4	Upper Threshold	Ch.11	R/W	170	Vcc Value, Bank 3	Ch.09-12	R
040	De-bounce time	Ch.03	R/W	0D8	Lower Threshold	Ch.11	R/W	174	Vcc Value, Bank 4	Ch.13-16	R
044	Max High Threshold	Ch.04	R/W	0DC	Min Low Threshold	Ch.11	R/W	178	Reset Over-Current	Ch.01-16	R/W
048	Upper Threshold	Ch.04	R/W	0E0	De-bounce time	Ch.11	R/W	18C	Module Design Version[1]		R
04C	Lower Threshold	Ch.04	R/W	0E4	Max High Threshold	Ch.12	R/W	190	Module Design Revision[1]		R
050	Min Low Threshold	Ch.04	R/W	0E8	Upper Threshold	Ch.12	R/W	194	Module DSP[1]		R
054	De-bounce time	Ch.04	R/W	0EC	Lower Threshold	Ch.12	R/W	198	Module FPGA[1]		R
058	Max High Threshold	Ch.05	R/W	0F0	Min Low Threshold	Ch.12	R/W	19C	Module ID		R
05C	Upper Threshold	Ch.05	R/W	0F4	De-bounce time	Ch.12	R/W	1A0	Status Fault	Ch.01-16	R
060	Lower Threshold	Ch.05	R/W	0F8	Max High Threshold	Ch.13	R/W	1A8	Status Over-Current	Ch.01-16	R
064	Min Low Threshold	Ch.05	R/W	0FC	Upper Threshold	Ch.13	R/W	1AC	Status Max Hi Threshold	Ch.01-16	R
068	De-bounce time	Ch.05	R/W	100	Lower Threshold	Ch.13	R/W	1B0	Status Min Lo Threshold	Ch.01-16	R
06C	Max High Threshold	Ch.06	R/W	104	Min Low Threshold	Ch.13	R/W	1B4	Status Mid Range	Ch.01-16	R
070	Upper Threshold	Ch.06	R/W	108	De-bounce time	Ch.13	R/W	1B8	Status Lo-Hi Transition	Ch.01-16	R
074	Lower Threshold	Ch.06	R/W	10C	Max High Threshold	Ch.14	R/W	1BC	Status Hi-Lo Transition	Ch.01-16	R
078	Min Low Threshold	Ch.06	R/W	110	Upper Threshold	Ch.14	R/W	1C0	Interrupt Fault Enable	Ch.01-16	R/W
07C	De-bounce time	Ch.06	R/W	114	Lower Threshold	Ch.14	R/W	1D8	Interrupt Over-Current Enable	Ch.01-16	R/W
080	Max High Threshold	Ch.07	R/W	118	Min Low Threshold	Ch.14	R/W	1DC	Interrupt Max Hi Threshold Enable	Ch.01-16	R/W
084	Upper Threshold	Ch.07	R/W	11C	De-bounce time	Ch.14	R/W	1E0	Interrupt Min Lo Threshold Enable	Ch.01-16	R/W
088	Lower Threshold	Ch.07	R/W	120	Max High Threshold	Ch.15	R/W	1E4	Interrupt Mid-Range Fault Enable	Ch.01-16	R/W
08C	Min Low Threshold	Ch.07	R/W	124	Upper Threshold	Ch.15	R/W	1E8	Interrupt Lo-Hi Transition Enable	Ch.01-16	R/W
090	De-bounce time	Ch.07	R/W	128	Lower Threshold	Ch.15	R/W	1EC	Interrupt Hi-Lo Transition Enable	Ch.01-16	R/w
094	Max High Threshold	Ch.08	R/W	12C	Min Low Threshold	Ch.15	R/W				

Note: 1. Pending

Write Output

When a channel is configured for Output, write logic level High (“1”) or Low (“0”) to associated channel bit, in 16 bit binary word. Each bit corresponds to one of 16 channels (See Register Bit Map.) Output logic is defined by the provided Vcc voltage to that channel bank. There are four channels per bank (See J1 & J2, or P2 & P0 pin out.)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

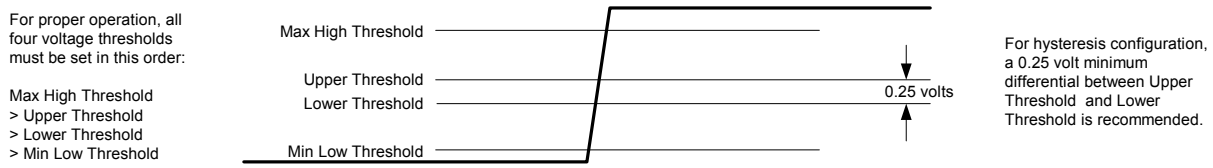
Read I/O

Independent of channel configuration (Input or Output), read logic state High (“1”) or Low (“0”) as defined by channel threshold values. Each bit of 16-bit binary word corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

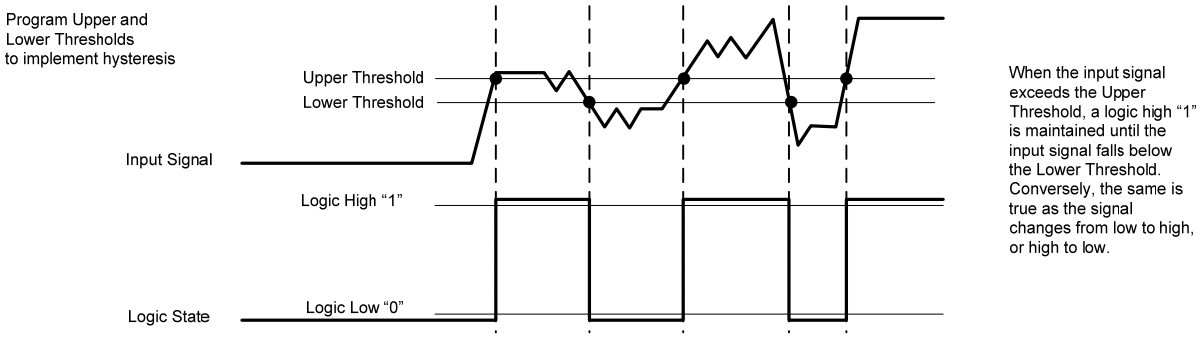
Threshold Programming

All four threshold levels must be programmed. For Input, threshold levels define logic. For output, threshold levels are used in BIT (wrap around) test signal monitoring. For proper operation, the threshold values should be programmed such that Max High > Upper > Lower > Min Low Threshold.



Hysteresis

Program Upper and Lower Thresholds to implement the required hysteresis and then add de-bounce time as required. When the input signal exceeds the Upper Threshold, a logic high “1” is maintained until the input signal falls below the Lower Threshold. Conversely, when the input signal falls below the Lower Threshold, a logic low “0” is maintained until the input signal rises above the Upper Threshold. A 0.25 volt minimum differential is recommended between the Upper and Lower Threshold values.



Max High Threshold

Maximum High Threshold is programmable per channel from 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv. Assumes that the programmed level is the minimum voltage used to indicate a Max HighThreshold. If a signal is greater then the Max High Threshold value, flag is set in the *Max High Threshold Status register*. The Max High Threshold register may be used to monitor any type of high signal voltage condition or threshold such as a “Short to +V” as it applies to input measurement as well as contact sensing applications.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
MAX HIGH THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

Upper Threshold

Upper Threshold is programmable per channel from 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv. A signal is considered logic High (“1”) when its value exceeds the Upper threshold and does not consequently fall below the Lower threshold in less than the programmed De-bounce time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
UPPER THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

Lower Threshold

Lower Threshold is programmable per channel from 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv. A signal is considered logic Low (“0”) when its value falls below the Lower threshold and does not consequently rise above the Upper Threshold in less than the programmed De-bounce time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
LOWER THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

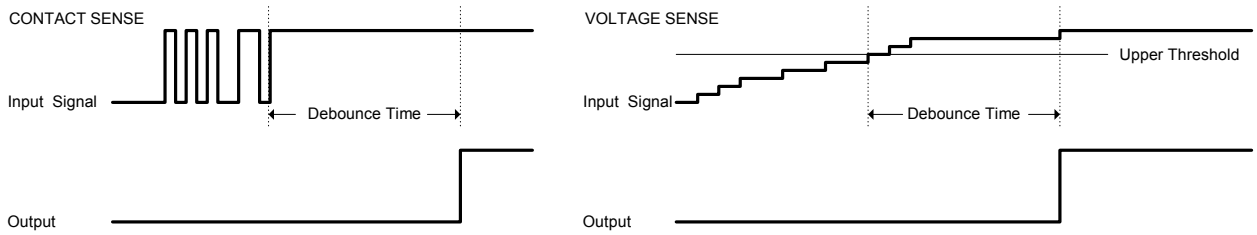
Min Low Threshold

Minimum Low Threshold is programmable per channel 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv**.** Assumes that the programmed level is the maximum voltage used to indicate a Min Low Threshold. If a signal is less then the Min Low Threshold value, a flag is set in the *Min Low Threshold Status register*. The Min Low Threshold register may be used to monitor any type of low signal voltage condition or threshold such as a “Short to Ground” as it applies to input measurement as well as contact sensing applications.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
MIN LOW THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

De-bounce time

Enter required de-bounce time into appropriate channel registers. Enter time in 20μs increments, up to 0.655 seconds. LSB= 20 μs. Value is 15 bits (MSB=don’t care). De-bounce defaults to 0 upon reset. For contact sensing, De-bounce time is much like a glitch filter. Signal pulse widths less than the De-bounce time are filtered or ignored. Once a signal level is stable for a period longer than the De-bounce time (see Upper and Lower Threshold described above), a logic transition is validated. For voltage sensing, the input signal level must exceed its associated threshold for a time greater then the De-bounce time for the logic transition to be validated (see Upper and Lower Threshold described above). Once valid, the interrupt transition register channel flag is set and the output logic changes state. Enter a value of 0 to disable De-bounce filtering.



REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
		~328	~164	~82	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	value in mSec (LSB=20μS)
DE-BOUNCE TIME	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

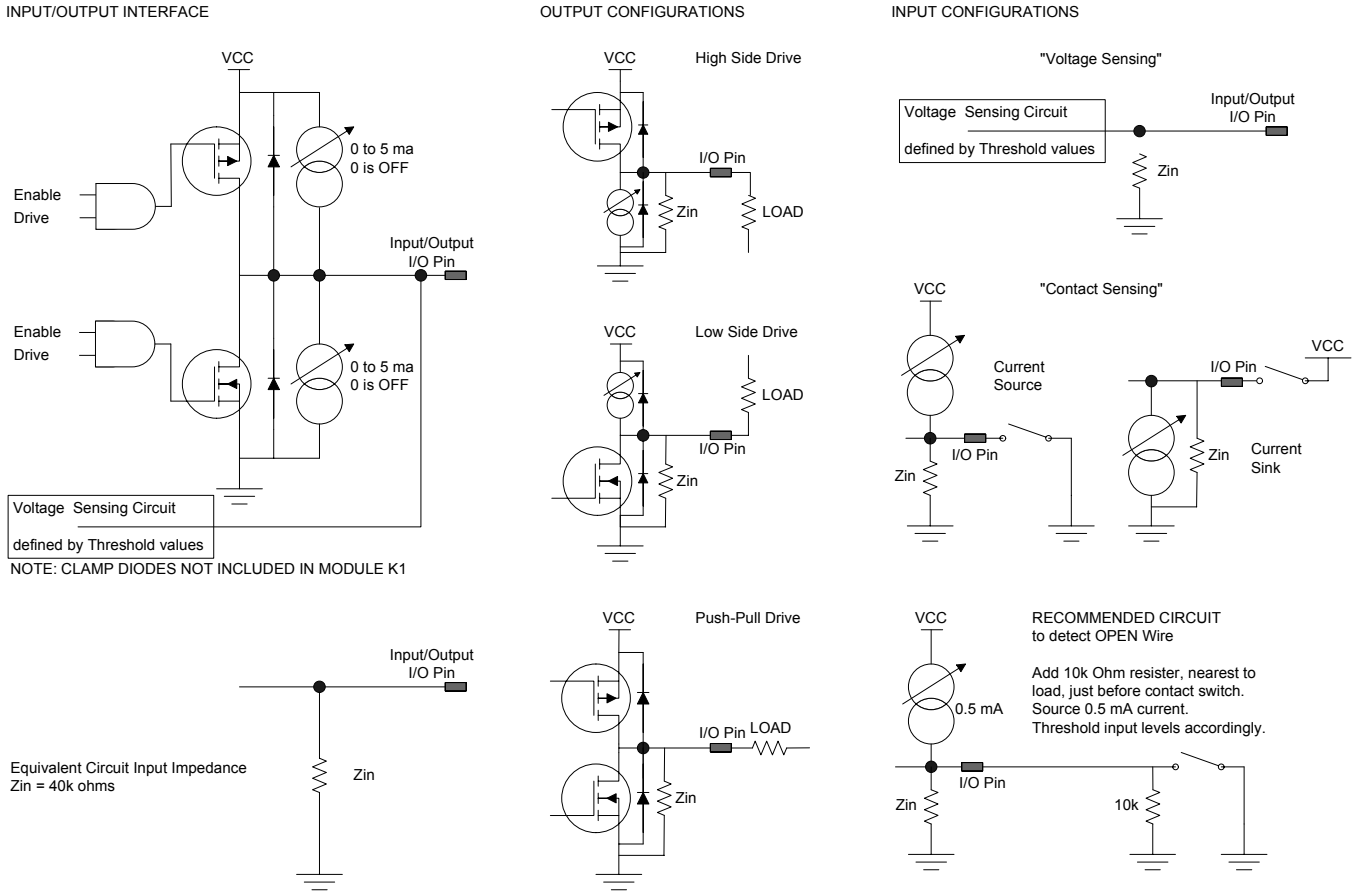
Input/Output Interface

The Input/Output (I/O) Interface can be configured in a variety of ways. A pair of drive FETs and current circuits are provided at each I/O pin. See I/O interface diagram below.

Output: When configured as an output, the interface can act as a "High-Side", "Low-Side" or "Push-Pull" drive, providing up to 500ma per channel. The total output per module (16 channels) cannot exceed 2 amps.

Input: When configured as an input, output drivers are disabled. I/O interface can act as a current source, current sink or voltage sensing circuit. For contact sensing, set each channel for pull-up or pull-down using the *Pull-Up/Down Current Configuration* register and enter the appropriate current level in the *Current For Sink/Source* register. Define contact closure and hysteresis using Upper and Lower Threshold. See *Read I/O* register to read input signal logic state. *No additional resistors or hardware is required to provide for current flow.* A current value of zero disables the current source/sink circuits and configures for voltage sensing. Default is voltage sensing.

All four threshold levels must be programmed. For input, threshold levels define logic state. For output, threshold levels are used in BIT test (wrap-around) signal monitoring.



To detect an OPEN line when **contact sensing,** add 10k ohm resistor R_{nl} nearest to load. Program open detect current I_{od} and calculate open contact condition, drop voltage V_{open} at I/O pin. Select sourcing current I_{od} such that drop voltage ΔV is about 80% of Vcc. If open detect resistance R_{od} is the parallel combination of the near load resistance R_{nl} and the circuit input impedance Z_{in}. Then

$R_{od} = R_{nl} \,||\, Z_{in} = 10k \,||\, 40k = 8k.$

If user provided Vcc is 10v,

$I_{od} = 0.8\ Vcc / R_{od} = 0.8 \times 10 / 8k = 1ma.$

If I_{od} = 1ma, we get open contact condition, drop voltage V_{open} at the I/O pin,

$V_{open} = I_{od}R_{od} = 1ma \times 8k\Omega = 8.0$ volts.

If load is current sink, Program Maximum Upper Threshold T_{mu}, some 20% greater then V_{open} , maintaining

$Vcc > T_{mu} > V_{open} > T_{ut}$,

T_{mu} = 1.2 V_{open} = 1.2 x 8 = 9.6 volts.

Program Upper Threshold T_{ut} 20% less then V_{open}

T_{ut} = 0.8 V_{open} = 0.8 x 8 = 6.4 volts.

Accordingly, program Lower Threshold T_{lt} at 20% Vcc and Minimum Lower Threshold T_{ml} at 10% Vcc

T_{lt} = 0.2 Vcc = 0.2 x 10 = 2 volts.
T_{ml} = 0.1 Vcc = 0.1 x 10 = 1 volts.

To detect a line SHORT when **contact sensing** and continuing with this example, user needs to add series resistance nearest to load, Rs and calculate closed contact condition, drop voltage V_{closed} at I/O pin. Resistance nearest to load, R_s should be negligible as compared to the near load resistance R_{nl} but at least a magnitude greater than any resistance due to wire length. A value of 150 ohms would be appropriate for Rs. Then

$V_{closed} = I_{od}R_s$ = 1ma x 0.1kΩ = 0.15 volts.

Program Lower Threshold T_{mu}, greater then V_{closed} maintaining

Vcc >> T_{lt} > V_{closed} > T_{ml} > 0

T_{lt} > 1.2 V_{closed} > 1.2 x 0.1 = 0.2 volts.

Program Minimum Lower Threshold T_{ut} 20% less then V_{open}

T_{ml} < 0.8 V_{closed} < 0.8 x 0.15 = 0.1 volts.

In general,

Vcc > T_{mu} > V_{open} > T_{ut},> T_{lt} > V_{closed} > T_{ml} > 0, $T_{ut} - T_{lt} \geq 0.25$mV for hysteresis configuration

To detect a Short to Vcc, Program Maximum Upper Threshold T_{mu}, where

Vcc > T_{mu} > $V_{loadmax}$, where $V_{loadmax}$ is the maximum voltage potential on the I/O pin.

To detect a Short to Ground, Program Minimum Lower Threshold T_{ml}, where

Vcc > > $V_{loadmin}$ > T_{ml}, where $V_{loadmin}$ is the minimum voltage potential on the I/O pin.

Consider the following programming options:

Output Programming Examples:

Figure	INPUT/OUTPUT FORMAT 2 bits per channel	Integer	PULL-UP/DOWN Configuration 1 bit per 4-channel bank	Integer	CURRENT FOR SOURCE/SINK One register per 4-channel bank	Integer
1	Output Ch1, High Side Drive	2	without current pull down	X	NO current source	0
1	Output Ch1-4, High Side Drive	170	Ch1-4 with current pull down[1]	14	1 ma	10
1	Output Ch5-8, High Side Drive	43520	Ch5-8 with current pull down[1]	13	2 ma	20
1	Output Ch1-8, High Side Drive	43690	Ch1-8 with current pull down[1]	12	2 ma	20
2	Output Ch1, Low Side Drive	1	without current pull up	X	NO current source	0
2	Output Ch1-4, Low Side Drive	85	Ch1-4 with current pull up[1]	1	1 ma	10
2	Output Ch1-8, Low Side Drive	21845	Ch1-8 with current pull up[1]	3	2 ma	20
3	Output Ch1, Push-Pull	3	Not Applicable – DON'T CARE	X	Not Applicable – DON'T CARE	X

Note 1: Use current source for Wired-OR or other related applications.

OUTPUT CONFIGURATIONS

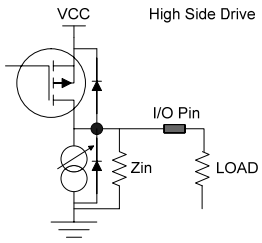


Figure 1

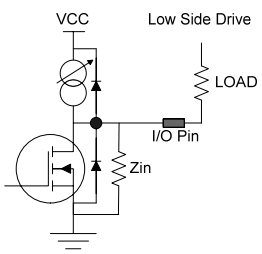


Figure 2

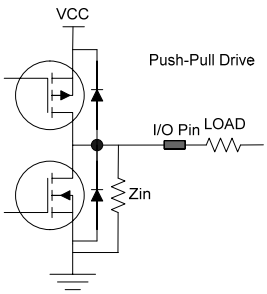


Figure 3

Input Programming Examples:

Figure	INPUT/OUTPUT FORMAT 2 bits per channel	Integer	PULL-UP/DOWN Configuration 1 bit per 4-channel bank	Integer	CURRENT FOR SOURCE/SINK One register per 4-channel bank	Integer
4	Input Ch1-8, voltage sensing (default)	0	without current source/sink	X	NO current source (default)	0
5	Input Ch1-8, contact sensing	0	Ch1-8 with current pull up	3	1 ma	10
6	Input Ch1-8, contact sensing	0	Ch1-8 with current pull down	12	2 ma	20
7	Input Ch1-8, OPEN line detect, load is current sink	0	Ch1-8 with current pull up	3	0.5 ma Program Max Upper Threshold[2]	5
6[1]	Input Ch1-8, OPEN line detect, load is current source	0	Ch1-8 with current pull down	12	0.5 ma Program Min Lower Threshold[3]	5

Notes 1. Figure 6 with 10k ohm resistor nearest load (as in figure 7)

2. $Vcc > T_{mu} > I_{od}R_{od}$, where load is current sinking

3. $T_{ml} < Vcc - I_{od}R_{od}$, where load is current sourcing

INPUT CONFIGURATIONS

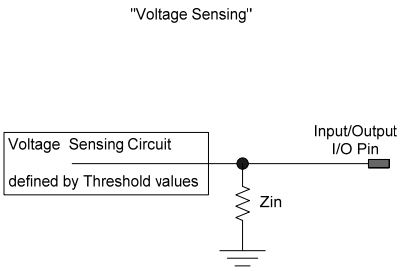


Figure 4

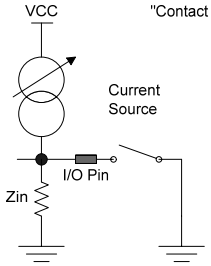


Figure 5

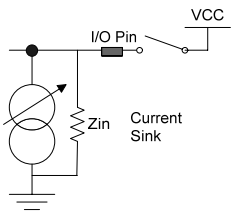


Figure 6

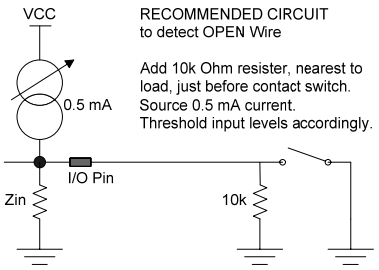


Figure 7

Current for Source/Sink

Program any current from 0 to 5 ma. Programs entire bank; there are 4 channels per bank. For 5ma, enter integer 50. Resolution is 100µa per bit (LSB=100µa). A current value of zero disables the current source/sink circuits and configures for voltage sensing.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
											3.2	1.6	0.8	0.4	0.2	0.1	value in mA (LSB=100µA)
CURRENT	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input/Output format

Configure channels in groups of 8. Write integer 0 for input, 1, 2 or 3 for output. While each channel may be programmed for either input or output individually, Pull-up/down Current Configuration must be programmed in four channel banks.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INPUT/OUTPUT CH 01-08	Ch.08		Ch.07		Ch.06		Ch.05		Ch.04		Ch.03		Ch.02		Ch.01		Channel
INPUT/OUTPUT CH 09-16	Ch.16		Ch.15		Ch.14		Ch.13		Ch.12		Ch.11		Ch.10		Ch.09		Channel
INPUT/OUTPUT	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT

Integer	D_H	D_L	
0	**0**	**0**	Input
1	**0**	**1**	Output, Low-side switched, with/without current pull up
2	**1**	**0**	Output, High-side switched, with/without current pull down
3	**1**	**1**	Output, push-pull

Pull-up/down Current Configuration

Set bit "1"=to configure Bank to Pull-up, or clear bit "0" to configure Bank to Pull-down. Each data bit configures entire bank of 4 channels. Defaults to "1"; pull-up configuration. Register data bits D4 through D15 are "don't care": XXXX XXXX XXXX $D_3D_2D_1D_0$

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
VCC VALUE	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	1=Pull-Up, 0=Pull-Down
D0 configures bank 1, channels 1-4 of that module.																**D**	Configure Ch.01-04
D1 configures bank 2, channels 5-8 of that module.															**D**		Configure Ch.05-08
D2 configures bank 3, channels 9-12 of that module.														**D**			Configure Ch.09-12
D3 configures bank 4, channels 13-16 of that module.													**D**				Configure Ch.13-16

Examples: Register value is integer:

Register Value	Data Bits			Channel Configuration, Module 1		
	D15-D2	**D1**	**D0**	Ch. 9-16	Ch. 5-8	Ch. 1-4
0	**0000 0000 0000 00 - -**	**0**	**0**	Pull-Down	Pull-Down	Pull-Down
1	**0000 0000 0000 00 - -**	**0**	**1**	Pull- Down	Pull-Down	Pull-Up
2	**0000 0000 0000 00 - -**	**1**	**0**	Pull- Down	Pull-Up	Pull-Down
3	**0000 0000 0000 00 - -**	**1**	**1**	Pull- Down	Pull-Up	Pull-Up

Vcc Value

Read Vcc voltage at input pin per four channel bank. Value is binary 10 bit word, where LSB=100 mv. Whether configured for input or output, user provided Vcc must be wired for proper operation.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1	value in volts (LSB=100mv)
VCC VALUE	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Reset Over-Current

Write integer "1" to reset all sixteen channels (per module). This register is used to reset disabled channel(s) set to tri-state following an over-current condition. When reset process is complete, processor will write a "0" back to the *Reset Over-Current* register. Card will respond to a Reset command after one second.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESET OVER-CURRENT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	D=DATA BIT

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4B31h

Read register to determine Module ID in ASCII. For example, find ASCII "K" in upper byte and ASCII "1" in lower byte for Module "K1," together 4B31h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "K"								ASCII "1"								

Automatic background BIT testing

BIT is always enabled and continually checks that each channel is functional. This capability is accomplished by an additional Test A/D that is incorporated into each 16 channel module. The Test A/D is sequentially connected across each channel and compared against the operational channel. Depending upon configuration, the Input data read or Output logic write of the operational channel and Test A/D must agree or a fault is indicated with the results available in the associated status register. Additional testing is provided to check for Over-current condition. *All four threshold levels must be set for each Input or Output channel to validate BIT testing*. The card will write 55h to the *Test (D2) Register*, every 30 seconds. User can periodically clear the *Test (D2) Register* by writing 00h, waiting 30 seconds then reading the register again to verify that background BIT testing is functioning. Testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and associated status register(s) can be checked or polled at any given time. Enable Interrupts, within any interrupt enable register, by setting the appropriate channel bits to 1.

Status indications

Fault – Channel processing (data read or write logic) is inconsistent with redundant test circuit. Status (bit is set) is indicated within 15 seconds. A fault is latched until read. (Testing takes approx. 1 second per channel)

Over-current – If over-current or overload condition is sensed, status is indicated (bit is set) within 80µs.
Max High Threshold – If the signal exceeds this threshold, status is indicated (bit is set) within 40µs.
Min Low Threshold – If the signal falls below this threshold, status is indicated (bit is set) within 40µs.
Lo-Hi Transition – If a Lo to High transition is sensed, status is indicated (bit is set) within 40µs.
Hi-Low Transition – If a High to Low transition is sensed, status is indicated (bit is set) within 40µs.
Mid-Range – When the signal is in-between the Upper and Lower thresholds, status is indicated (bit set) within 40µs.

When status is "indicated," or bit is "set," bit value is logic "1." Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Max Hi Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Min Lo Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Mid-Range	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Max Hi Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Min Lo Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Mid-Range Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

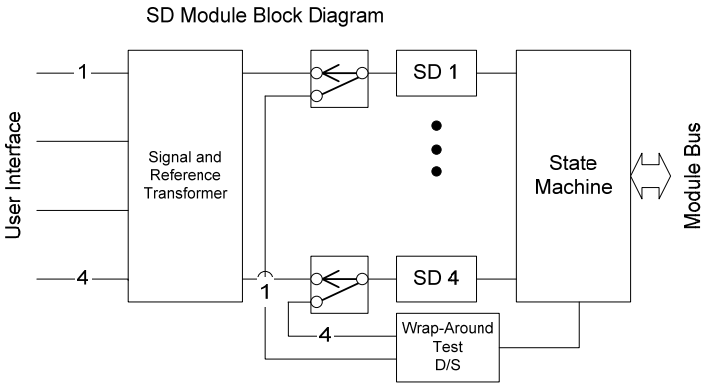
Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored.

When status is “indicated,” or bit is “set,” bit value is logic “1.” Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Max Hi Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Min Lo Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Mid-Range	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Max Hi Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Min Lo Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Mid-Range Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

S/D (MODULE S)



This S/D measurement design has the capability to automatically shift to higher bandwidths when high acceleration events are encountered. There is not data latency. The shifting is smooth and continuous with no glitches. Tracking rates are only limited to bandwidth restrictions, up to 150 RPS, at 16-bit resolution. Both a software and hardware LATCH feature is provided to permit the user to read all channels at the same time. Reading will unlatch that channel. The angle alert monitors each channel for the programmed angle difference and sets an interrupt as soon as that threshold is reached. Thus, no polling of the angle registers is required until an angle has reached the specified difference. The use of Type II servo loop processing techniques enables tracking, at full accuracy, up to the specified rate. A step input will not cause any hang-up condition. Intermediate transparent latches, on all angle and velocity outputs, assure that valid data is always available. Our synthetic reference compensates for ±60° phase shifts, thus eliminating the need for individual compensation networks.

The (D2) Test initiates automatic background BIT testing. Each channel is checked every 5° to a testing accuracy of 0.05° and each Signal and Reference is always monitored. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled via the bus.

The (D3) Test initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. Results can be read from registers and external reference is not required. Any failure triggers an Interrupt (if enabled). The testing requires no external programming, and can be initiated or stopped via the bus.

The (D0) Test is used to check the card and the cPCI interface. All channels are disconnected from the outside world, allowing the user to write any number of input angles to the card and then to read the data from the interface. External reference is not required.

NOTE: Special consideration must be exercised when Synchro/Resolver (S/R) or LVDT/RVDT (L/R) measurement functions are required. In either case, if S/R or L/R measurement is required, slots 4, 5 and 6 must be dedicated to that particular function. S/R or L/R measurement cannot be mixed together, or mixed with any other module type. For 4 channel requirements, slot 4 will be populated. For 8 channel requirements, slot 4 and 5 will be populated. The remaining third slot must remain unused. The other three slots 1 2 and 3 can be used for a mix of A/D, D/A, I/O or other, but never S/R or L/R function.

S/D (FIXED SLOTS 4, 5 AND 6) MEMORY MAP

600	Ch.1 Data Hi	R	674	D0 Test Angle	W	6F0	Reference Frequency	R/W
604	Ch.2 Data Hi	R	678	Two-Speed Lock-Loss	R	6F4	Reference Voltage	R/W
608	Ch.3 Data Hi	R	67C	Synchro / Resolver	R/W	700	Ch.2 Data Lo	R
60C	Ch.4 Data Hi	R	680	Active Channels	R/W	704	Ch.4 Data Lo	R
610	Ch.5 Data Hi	R	68C	Latch	W	708	Ch.6 Data Lo	R
614	Ch.6 Data Hi	R	690	Ch.1 Velocity Scale	R/W	70C	Ch.8 Data Lo	R
618	Ch.7 Data Hi	R	694	Ch.2 Velocity Scale	R/W	78C	Module Design Version[1]	R
61C	Ch.8 Data Hi	R	698	Ch.3 Velocity Scale	R/W	790	Module Design Revision[1]	R
620	Ch.1 Velocity	R	69C	Ch.4 Velocity Scale	R/W	794	Module DSP[1]	R
624	Ch.2 Velocity	R	6A0	Ch.5 Velocity Scale	R/W	798	Module FPGA[1]	R
628	Ch.3 Velocity	R	6A4	Ch.6 Velocity Scale	R/W	79C	Module ID Slot 4	R
62C	Ch.4 Velocity	R	6A8	Ch.7 Velocity Scale	R/W	7A0	BIT Status Ch.1-8	R
630	Ch.5 Velocity	R	6AC	Ch.8 Velocity Scale	R/W	7A4	Signal Status Ch.1-8	R
634	Ch.6 Velocity	R	6B0	(A & B) res. Ch.1	R/W	7A8	Reference Status Ch.1-8	R
638	Ch.7 Velocity	R	6B4	(A & B) res. Ch.2	R/W	7AC	Angle Δ Alert Ch.1-8	R
63C	Ch.8 Velocity	R	6B8	(A & B) res. Ch.3	R/W	7D0	BIT Status Interrupt Enable Ch.1-8	R/W
640	Ratio Ch.2 / Ch.1	R/W	6BC	(A & B) res. Ch.4	R/W	7D4	Signal Status Interrupt Enable Ch.1-8	R/W
644	Ratio Ch.3 / Ch.4	R/W	6C0	(A & B) res. Ch.5	R/W	7D8	Reference Status Intr Enable Ch.1-8	R/W
648	Ratio Ch.5 / Ch.6	R/W	6C4	(A & B) res. Ch.6	R/W	7DC	Angle Δ Alert Interrupt Enable Ch.1-8	R/W
64C	Ratio Ch.7 / Ch.8	R/W	6C8	(A & B) res. Ch.7	R/W	98C	Module Design Version	R
650	Ch.1 Angle Δ	R/W	6CC	(A & B) res. Ch.8	R/W	990	Module Design Revision	R
654	Ch.2 Angle Δ	R/W	6D0	Reserved		994	Module DSP	R
658	Ch.3 Angle Δ	R/W	6D4	Reserved		998	Module FPGA	R
65C	Ch.4 Angle Δ	R/W	6D8	Reserved		99C	Module ID Slot 5	R
660	Ch.5 Angle Δ	R/W	6DC	Reserved		B8C	Module Design Revision	R
664	Ch.6 Angle Δ	R/W	6E0	Reserved		B90	Module Design Revision	R
668	Ch.7 Angle Δ	R/W	6E4	Reserved		B94	Module DSP	R
66C	Ch.8 Angle Δ	R/W	6E8	Reserved		B98	Module FPGA	R
670	Angle Init	R/W	6EC	Reserved		B9C	Module ID Slot 6	R

Note: 1. Pending

Data

Date Hi Type: 16 bit unsigned integer
Date Hi & Lo Type: 24 bit unsigned integer (Multi-Speed Applications)
Range: 0 to 359.9945 degrees
Read/Write: R

For Single Speed (Ratio=1) applications, read *Data High* register of that channel. For Multi-Speed applications, read *Data High* register of the even channel (2 or 4) for that pair where 16-bit resolution is required. LSB is approximately 0.0055 degrees.

For better than 16-bit resolution Multi-Speed requirements, use *Data High* and *Data Low* registers combined to determine measured angle with up to 24-bit resolution. First read *Data High* word, then *Data Low* word. Data high word, when read, latches low word. Data Low word, when read, unlatches data. LSB is dependant upon Ratio. A gear ratio of 256 provides for a 24-bit resolution, a ratio of 128 provides for a 23-bit resolution, and so on.. The N-speed information (Multi-Speed, Fine) from the synchro should be connected to the even channel of that pair. The pairs are defined as Ch.1 & 2 and Ch.3 & 4. NOTE: Per bit angle values in below table are approximate.

DATA HIGH REGISTER																DATA LOW REGISTER															
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	X	X	X	X	X	X	X	X

Velocity

Type: 16 bit 2's complement word
Range: 0x7FFF maximum CW rotation to 0x8000 maximum CCW
Read/Write: R
Initialized Value: N/A

Read Velocity Registers of each channel as a 2's complement word, with 7FFFh being maximum CW rotation, and 8000h being maximum CCW rotation.

When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CW would be read as 0863h.
When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CCW would be read as F79Ch.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CW would be read as 192Ah.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CCW would be read as E6D5h.

To convert a velocity word to RPS: **Velocity in RPS = Maximum x Output / Full Scale**

If Velocity Output were E6D5h, and maximum velocity were 50.8626 RPS, then

Velocity in RPS = 50.8626 x E6D5h / 32,768 = 50.8626 x -6,442 / 32,768 = -10 RPS

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
VELOCITY	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT, 2's Complement

Ratio

Type: 16 bit unsigned integer
Range: 1 to 255
Read/Write: R/W
Initialized Value: 1 (Single-Speed)

Enter the desired ratio, as an integer number, in the *Ratio* Register corresponding to the pair of channels to be used for a two-speed, or multi-speed configuration. Example, 36:1 = integer 36. Default is for single speed applications where Ratio = 1.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RATIO	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Angle Δ

Type: 16-bit unsigned integer
Range: 0.05 to 180 degrees
Read/Write: R/W
Initialized Value: 0

Enter the minimum differential angle to associated channel *Angle Δ* register required to trigger an angle change alert. See *Angle Δ Alert* register description for details. MSB=180°; minimum differential is 0.05°.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	approximate value
ANGLE Δ	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Degrees)

Angle Δ Initiate

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Set the bit corresponding to each channel to be monitored for angle change alert. Set bit to "1" for monitoring channels and clear bit to "0" for those not used.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE INTIATE	X	X	X	X	X	X	X	X	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	CHANNEL ENABLE BIT

Active Channels

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Set the bit corresponding to each channel to be monitored during BIT testing in the *Active Channel* register. Set bit to "1" for active channels and clear bit to "0" for those not used. Omitting this step will produce false alarms, because unused channels will set faults.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ACTIVE CHANNEL	X	X	X	X	X	X	X	X	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	CHANNEL ENABLE BIT

Latch

Type: 16 bit unsigned integer
Range: 0 or 2
Read/Write: R
Initialized Value: 0

Writing the integer 2 to the *Latch* register will cause all the channels to be latched. Reading a particular channel will disengage the latch for that channel. Writing a 0 to this register will disengage latch on all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
LATCH	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Test Angle

Type: 16-bit unsigned integer
Range: 0 to 359.9945 degrees
Read/Write: W
Initialized Value: 30°

Enter the D0 test angle as per table.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	approximate value
TEST ANGLE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Degrees)

Two Speed Lock-Loss

Type: binary word
Range: N/A
Read/Write: R
Initialized Value: N/A

When two Synchros are geared to each other, either electrically or mechanically, in order to achieve higher accuracy the misalignment of the Coarse and Fine Synchros must not exceed 90°/gear ratio or the digital angle output may not be valid. Should this problem occur within a given channel pair, the corresponding bit in the *Two-Speed Lock-Loss* register will be set to "0".

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
LATCH	X	X	X	X	X	X	X	X	X	7/8	X	5/6	X	¾	X	½	CHANNEL PAIR

Velocity Scale

Type: 16 bit unsigned integer
Range: 9.5367 RPS to 152.5878 RPS
Read/Write: R/W
Initialized Value: N/A

The velocity scale factor is used to achieve a greater resolution at lower rotational speeds (RPS). The scale factor is: **4095(152.5878RPS/max RPS),** where the max RPS is selected by the user to achieve the maximum resolution for a desired RPS. Enter the scale factor as an integer to the corresponding *Velocity Scale* register for that particular channel.

To scale the Max Velocity word for 152.5878 RPS, set Velocity Scale Factor = 4095 (max velocity word of +32,767 (7FFFh) being 152.5878 RPS for CW rotation, and -32,768 (8000h) being 152.5878 RPS for CCW rotation). Scaling effects only the Velocity output word and not the dynamic performance.

To get a maximum velocity word (32,767) @ 152.5878 RPS, Scale Factor = 4095(152.5878/152.5878) = 4095 = 0FFFh;
This results in a velocity resolution of: (152.5878 RPS/32,767) x 360°/RPS = 1.676°/sec (factory default)

To get a maximum velocity word (32,767) @ 50.8626 RPS, Scale Factor = 4095(152.5878/50.8626) = 12,285 = 2FFDh);
This is a velocity resolution of: (50.8626 RPS/32,767) x 360°/RPS = 0.5588°/sec

For 9.5367 RPS max, Scale Factor = 4095(152.5878/9.5367) = 65,520 = FFF0h; 0.10477 °/sec res. (lowest setting)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
VELOCITY SCALE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

A & B Resolution

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Individually configure encoder output resolution or commutation for each channel.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
A & B RESOLUTION	D	X	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D=DATABIT
Integer 0	0													0	0	0	16 bit Encoder Resolution
Integer 1	0													0	0	1	15 bit Encoder Resolution
Integer 2	0													0	1	0	14 bit Encoder Resolution
Integer 3	0													0	1	1	13 bit Encoder Resolution
Integer 4	0													1	0	0	12 bit Encoder Resolution
Integer 32768	1													0	0	0	4 Pole Commutation
Integer 32769	1													0	0	1	6 Pole Commutation
Integer 32770	1													0	1	0	8 Pole Commutation

Synchro / Resolver

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Individually configure each channel for Synchro=1 or Resolver=0 measurement.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SYNCHRO / RESOLVER	X	X	X	X	X	X	X	X	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	CHANNEL BIT

Reference Frequency

Type: 16-bit unsigned integer
Range: 360 to 10,000 Hz
Read/Write: R/W
Initialized Value: N/A (S/R or L/R module Dependant)

Program Reference Frequency, where LSB is 1 Hz. For Example, 400 Hz = 0000 0001 1001 0000. Reference Module is Optional.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	-	8192	4096	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	approximate value
FREQUENCY	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)

Reference Voltage

Type: 16-bit unsigned integer
Range: 2.0 to 28.0 Vrms
Read/Write: R/W
Initialized Value: N/A (S/R or L/R module Dependant)

Program Reference Voltage, where LSB is 0.1 Vrms. For Example, 26.1 Vrms = 0000 0001 0000 0101. Reference Module is Optional.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	-	-	-	-	-	-	-	25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	approximate value
VOLTAGE	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Vrms)

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1"								ASCII " "								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "B"								ASCII " "								

Module DSP

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 5331h

Read register to determine Module ID in ASCII. For example, find ASCII "S" in upper byte and ASCII "1" in lower byte, for Module "S1," together 5331h. Slot 4 will be populated with an "S1" module for 4 or 8 channel applications. Slot 5 will be populated with an "S1" only in 8 channel applications. Slot 6 will be unused "Z0".

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "S"								ASCII "1"								

BIT Status

Type: binary word
Range: 0 to 15
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Built-In-Test (BIT) Status. Channel Status Data bit (Chn, where n is 1, 2, 3 or 4) is fail, high true, and indicates that the channel is not operating spec compliant. Status is latched. Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS	X	X	X	X	X	X	X	X	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Signal Status

Type: binary word
Range: N/A
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Signal Status. Status data bit is fail high true and indicates each a Signal input loss to that channel. Signal Loss is indicated after 2 seconds. Signal input monitoring is disabled during D3 or D0 Test. Any Signal Status failure, transient or intermittent will latch the *Signal Status* register. Reading any status bit will unlatch the entire register. Signal Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Open Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS	X	X	X	X	X	X	X	X	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Reference Status

Type: binary word
Range: N/A
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Reference Status. Status data bit is fail high true and indicates each a Reference input loss to that channel. Signal and/or Reference Loss is indicated after 2 seconds. Signal and Reference input monitoring is disabled during D3 or D0 Test. Any Reference Status failure, transient or intermittent will latch the *Reference Status* register. Reading any status bit will unlatch the entire register. Reference Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Over-Current Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
REFERENCE STATUS	X	X	X	X	X	X	X	X	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Angle Δ Alert

Type: binary word
Range: 0 to 15
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Angle Δ Alert Status. Angle Δ Alert Status Data bit (Chn, where n is 1 to 8) is fail, high true, and indicates that the angle position of that channel has exceeded the minimum differential angle specified in the *Angle Δ* register. Status is latched. Reading any status bit will unlatch the entire register. Angle Change Alert part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Max-Hi Threshold Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE Δ ALERT	X	X	X	X	X	X	X	X	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

BIT Status Interrupt Enable

Type: binary word
Range: 0 to 15
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 0 to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS INTR ENA	X	X	X	X	X	X	X	X	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

Signal Status Interrupt Enable

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal (open) status (signal or reference input loss) will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Open Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS INTERRUPT ENABLE	X	X	X	X	X	X	X	X	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

Reference Status Interrupt Enable

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal (open) status (signal or reference input loss) will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Over-Current Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
REFERENCE STATUS INTERRUPT ENABLE	X	X	X	X	X	X	X	X	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

Angle Δ Alert Interrupt Enable

Type: binary word
Range: 0 to 15
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, an angle Δ alert will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Max-Hi Threshold Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE Δ INTR ENA	X	X	X	X	X	X	X	X	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

GENERAL USE REGISTER MEMORY MAP

The registers of this memory map apply to the complete card. The *Test Enable* and related registers affect all modules unless otherwise specified. BIT tests are module dependant. See module description for details.

MEMORY MAP

C00	Part number	R	C3C	Latch All A/Ds[1]	R/W
C04	Serial number	R	C40	A/D D0 Test Range[1]	R/W
C08	Date Code	R	C44	A/D D0 Test Voltage[1]	R/W
C0C	Rev. Level, PCB	R	C48	D/A Reset to Zero[2]	R/W
C10	Rev. Level, Processor 1	R	C4C	D/A Retry Overload[2]	R/W
C14	Rev. Level, Processor 2	R	C50	D/A Reset Overload[2]	R/W
C18	Rev. Level, PCI FPGA	R	C54	D/A Override[2]	R/W
C1C	Rev. Level, FPGA 1	R	C60	Design Version	R
C20	Rev. Level, FPGA 2	R	C64	Platform	R
C24	Board Ready	R	C68	Model	R
C28	Watchdog Timer	R/W	C6C	Generation	R
C2C	Soft reset	W	C70	Special Spec	R
C30	Test Enable	R/W	C74	Interrupt Status	R
C34	Test (D2) verify	R/W	C78	Interrupt Clear	R/W

Address to General Use Registers has NO MODULE OFFSET.

Note: 1. Only affects A/D Modules.
2. Only affects D/A Modules.

Part Number

is read as a 16 bit binary word. A unique 16 bit code is assigned to each model number.

Serial Number

is read as a 16 bit binary word.

Date Code

Read as a decimal number. The four digits represent YYWW (Year, Year, Week, Week)

Revisions

Read as a 16 bit binary word

Board Ready

Poll register. Board is ready to be accessed **only after** you read “AA55”. (within 1 second after board power-on)

Watchdog timer

This feature monitors the watchdog timer register. When it detects that a code has been received, that code will be inverted within 100 µSec. The inverted code stays in the register until replaced by a new code. After 100 µSec. elapse, look for the inverted code to confirm that the processor is operating.

Soft reset

Soft Reset is Level sensitive. Writing a “1” initiates and holds software in reset state; then writing “0” initiates reboot (depending upon configuration, takes up to 3 seconds). This function is equivalent to a power-on reset where all parameters are reset to their default condition.

Test Enable

Set bit to enable associated Built-In Self Test D3, D2, or D0. Each test affects each Module Type differently. See the individual module section for test description(s).

Write “1” to D2 to initiate automatic background BIT testing. Card will (every 30 seconds) write 55h at *Test (D2) verification* register when D2 is enabled. User can periodically clear to 00h and then read *Test (D2) verification* register again, after 30 seconds, to verify that background bit testing is activated. D3 test cycle is completed within 45 seconds and results can be read from the associated status registers when D3 changes from “1” to “0”. Any

failure triggers an Interrupt (if enabled). All testing requires no external programming and is initiated by writing “1” or terminated by writing “0”.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0

Test (D2) Verify

Card will (every 30 seconds) write 55h at *Test (D2) Verification* register when (D2) is enabled. User can periodically clear to 00h and then read again, after 30 seconds, to verify that background bit testing is activated.

Latch All A/Ds

Latch all A/D channels by writing “1” to D1 of Latch register. Write “0” to unlatch all channels.

A/D D0 Test Range

Specify voltage range for A/D module under test. D0 test is performed only on A/D modules. Enter per table:

A/D	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D0 Test Range	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D	D

Range					
40.0 V	∗	1	0	1	0
20.0 V	∗	1	0	0	1
10.0 V	∗	0	0	0	0
5.00 V	∗	0	0	0	1
2.50 V	∗	0	0	1	0
1.25 V	∗	0	0	1	1
0.625 V	∗	0	1	0	0

∗ For bipolar/unipolar selection, program D4 as “0” for unipolar and “1” for bipolar.

A/D D0 Test Voltage

Specify voltage to be applied by D0 test to A/D module under test. D0 test is performed only on A/D modules. If using bi-polar mode, write 16 bit 2’s complement word (7FFFh=+FS, 8000h=-FS). If using uni-polar mode, write 16 bit binary word (range: 0 to FFFFh=FS).

Example 1: if using uni-polar mode with 10v range, enter 8000h for 5v test voltage.
Example 2: if using bi-polar mode with 10v range, enter 4000h for 5v test voltage. Enter C000h for –5v.

D/A Reset to Zero

Write “1” to drive all D/A outputs to zero. When complete, *D/A Reset to Zero* register will be automatically set to “0”.

D/A Retry Overload

Write “1” to *D/A Retry overload* register to enable all channels (board wide) whose outputs were previously set to zero because of an overload condition. If and overload condition still exists, the channel output(s) will again be set to zero. While enabled, all overloaded channel outputs will be again be reset approximately every second. Default is “0”.

D/A Reset Overload

This register is used to reset all channels whose outputs were previously set to zero because of an overload. If an overload condition still exists, channel output(s) will again be set to zero. Channel output reset will occur one time only. *D/A Reset overload* register is be automatically reset to 0 after channel output reset activity is complete. Card will attempt to reset channel output(s) once for every time “1” is written to the register.

D/A Override

Write “1” at *Override* register to turn ON all overloaded outputs, short life condition.

Design Version

The register holds product design version in ASCII. For example, design version 1 would be ASCII "1" is in upper byte and ASCII "space" in lower byte, together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODEL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1 "								ASCII " "								

Platform

This register holds CPCI (6U) platform code "78" in ASCII. Find ASCII "7" is in upper byte and ASCII "8" in lower byte, together 3738h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PLATFORM	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "7"								ASCII "8"								

Model

The register holds product model code "C " in ASCII. Find ASCII "C" is in upper byte and ASCII "space" in lower byte, together 4320h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODEL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "C"								ASCII ""								

Generation

This register holds product generation code "1 " in ASCII. Find ASCII "1" is in upper byte and ASCII "space" in lower byte, together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
GENERATION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1"								ASCII ""								

Special Spec

This register holds product special specification code in ASCII. Find ASCII space used for none where ASCII "space" is in upper and lower bytes, together 2020h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt Status

Poll this register to determine interrupt status. Logic "1" indicates interrupt service is required; logic "0" indicates no interrupt requires servicing.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt Clear

Use this register to clear interrupt; usually cleared by user interrupt service routine. Enter logic "1" to indicate interrupt service complete. Register is cleared to logic "0" by the processor to acknowledge interrupt removal.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

FRONT AND REAR PANEL CONNECTORS

Front Panel Connectors J6 & J7 (AMP 748483-5; Mate AMP 748368-1), Rear Panel Connectors J3, J4 and J5.

DO NOT CONNECT TO ANY UNDESIGNATED (NC) PINS

REFERENCE OUTPUT

Front Panel, for Synchro/Resolver Measurement: Rhi Out J6 pin 33, Rlo Out J6 pin 72.
Rear Panel, for Synchro/Resolver Measurement: Rhi Out J5 pin E16, Rlo Out J5 pin E15.

SLOT 1

J7	J4	AD/DA	DA (J7)	RTD	Discrete	TTL	Signal	S/D	Differential
1	A1	M1Ch01 H	M1Ch01 H	M1Ch01 EX H	M1Ch01	M1Ch01	NC	M1Ch01 S1	M1Ch01 H
21	A2	M1Ch01 L	M1Ch01 L	M1Ch01 EX L	M1Ch02	M1Ch02	NC	M1Ch01 S3	M1Ch01 L
2	A3	M1Ch02 H	NC	M1Ch01 Sig H	M1Ch03	M1Ch03	NC	M1Ch01 S2	M1Ch02 H
22	A4	M1Ch02 L	NC	M1Ch01 Sig L	M1Ch04	M1Ch04	NC	M1Ch01 S4	M1Ch02 L
3	A5	M1Ch03 H	NC	M1Ch02 EX H	M1Vcc1-4	NC	NC	M1Ch01 RH	M1Ch03 H
23	A6	M1Ch03 L	NC	M1Ch02 EX L	M1Gnd1-4	NC	NC	M1Ch01 RL	M1Ch03 L
4	B1	M1Ch04 H	M1Ch02 H	M1Ch02 Sig H	M1Ch05	M1Ch05	M1Ch01	M1Ch02 S1	M1Ch04 H
24	B2	M1Ch04 L	M1Ch02 L	M1Ch02 Sig L	M1Ch06	M1Ch06	GND	M1Ch02 S3	M1Ch04 L
5	B3	M1Ch05 H	NC	M1Ch03 EX H	M1Ch07	M1Ch07	NC	M1Ch02 S2	M1Ch05 H
25	B4	M1Ch05 L	NC	M1Ch03 EX L	M1Ch08	M1Ch08	NC	M1Ch02 S4	M1Ch05 L
6	B5	AGND/NC	NC	M1Ch03 Sig H	M1Vcc5-8	NC	M1Ch02	M1Ch02 RH	M1Ch06 H
26	B6	NC	NC	M1Ch03 Sig L	M1Gnd5-8	NC	GND	M1Ch02 RL	M1Ch06 L
40	C1	M1Ch06 H	M1Ch03 H	M1Ch04 EX H	M1Ch09	M1Ch09	NC	M1Ch03 S1	M1GND
60	C2	M1Ch06 L	M1Ch03 L	M1Ch04 EX L	M1Ch10	M1Ch10	NC	M1Ch03 S3	M1GND
41	C3	M1Ch07 H	NC	M1Ch04 Sig H	M1Ch11	M1Ch11	M1Ch03	M1Ch03 S2	M1Ch07 H
61	C4	M1Ch07 L	NC	M1Ch04 Sig L	M1Ch12	M1Ch12	GND	M1Ch03 S4	M1Ch07 L
42	C5	M1Ch08 H	NC	M1Ch05 EX H	M1Vcc9-12	NC	NC	M1Ch03 RH	M1Ch08 H
62	C6	M1Ch08 L	NC	M1Ch05 EX L	M1Gnd9-12	NC	NC	M1Ch03 RL	M1Ch08 L
43	D1	M1Ch09 H	M1Ch04 H	M1Ch05 Sig H	M1Ch13	M1Ch13	M1Ch04	M1Ch04 S1	M1Ch09 H
63	D2	M1Ch09 L	M1Ch04 L	M1Ch05 Sig L	M1Ch14	M1Ch14	GND	M1Ch04 S3	M1Ch09 L
44	D3	M1Ch10 H	NC	M1Ch06 EX H	M1Ch15	M1Ch15	NC	M1Ch04 S2	M1Ch10 H
64	D4	M1Ch10 L	NC	M1Ch06 EX L	M1Ch16	M1Ch16	NC	M1Ch04 S4	M1Ch10 L
45	D5	NC	NC	M1Ch06 Sig H	M1Vcc13-16	NC	NC	M1Ch04 RH	M1Ch11 H
65	D6	NC	NC	M1Ch06 Sig L	M1Gnd13-16	NC	NC	M1Ch04 RL	M1Ch11 L

SLOT 2

J7	J4	AD/DA	DA (J7)	RTD	Discrete	TTL	Signal	S/D	Differential
27	A9	M2Ch01 H	M2Ch01 H	M2Ch01 EX H	M2Ch01	M2Ch01	NC	M2Ch01 S1	M2Ch01 H
8	A10	M2Ch01 L	M2Ch01 L	M2Ch01 EX L	M2Ch02	M2Ch02	NC	M2Ch01 S3	M2Ch01 L
28	A11	M2Ch02 H	NC	M2Ch01 Sig H	M2Ch03	M2Ch03	NC	M2Ch01 S2	M2Ch02 H
9	A15	M2Ch02 L	NC	M2Ch01 Sig L	M2Ch04	M2Ch04	NC	M2Ch01 S4	M2Ch02 L
29	A16	M2Ch03 H	NC	M2Ch02 EX H	M2Vcc1-4	NC	NC	M2Ch01 RH	M2Ch03 H
10	A17	M2Ch03 L	NC	M2Ch02 EX L	M2Gnd1-4	NC	NC	M2Ch01 RL	M2Ch03 L
30	B9	M2Ch04 H	M2Ch02 H	M2Ch02 Sig H	M2Ch05	M2Ch05	M2Ch01	M2Ch02 S1	M2Ch04 H
11	B10	M2Ch04 L	M2Ch02 L	M2Ch02 Sig L	M2Ch06	M2Ch06	GND	M2Ch02 S3	M2Ch04 L
31	B11	M2Ch05 H	NC	M2Ch03 EX H	M2Ch07	M2Ch07	NC	M2Ch02 S2	M2Ch05 H
12	B15	M2Ch05 L	NC	M2Ch03 EX L	M2Ch08	M2Ch08	NC	M2Ch02 S4	M2Ch05 L
32	B16	AGND/NC	NC	M2Ch03 Sig H	M2Vcc5-8	NC	M2Ch02	M2Ch02 RH	M2Ch06 H
13	B17	NC	NC	M2Ch03 Sig L	M2Gnd5-8	NC	GND	M2Ch02 RL	M2Ch06 L
66	C9	M2Ch06 H	M2Ch03 H	M2Ch04 EX H	M2Ch09	M2Ch09	NC	M2Ch03 S1	M2GND
47	C10	M2Ch06 L	M2Ch03 L	M2Ch04 EX L	M2Ch10	M2Ch10	NC	M2Ch03 S3	M2GND
67	C11	M2Ch07 H	NC	M2Ch04 Sig H	M2Ch11	M2Ch11	M2Ch03	M2Ch03 S2	M2Ch07 H
48	C15	M2Ch07 L	NC	M2Ch04 Sig L	M2Ch12	M2Ch12	GND	M2Ch03 S4	M2Ch07 L
68	C16	M2Ch08 H	NC	M2Ch05 EX H	M2Vcc9-12	NC	NC	M2Ch03 RH	M2Ch08 H
49	C17	M2Ch08 L	NC	M2Ch05 EX L	M2Gnd9-12	NC	NC	M2Ch03 RL	M2Ch08 L
69	D9	M2Ch09 H	M2Ch04 H	M2Ch05 Sig H	M2Ch13	M2Ch13	M2Ch04	M2Ch04 S1	M2Ch09 H
50	D10	M2Ch09 L	M2Ch04 L	M2Ch05 Sig L	M2Ch14	M2Ch14	GND	M2Ch04 S3	M2Ch09 L
70	D11	M2Ch10 H	NC	M2Ch06 EX H	M2Ch15	M2Ch15	NC	M2Ch04 S2	M2Ch10 H
51	D15	M2Ch10 L	NC	M2Ch06 EX L	M2Ch16	M2Ch16	NC	M2Ch04 S4	M2Ch10 L
71	D16	NC	NC	M2Ch06 Sig H	M2Vcc13-16	NC	NC	M2Ch04 RH	M2Ch11 H
52	D17	NC	NC	M2Ch06 Sig L	M2Gnd13-16	NC	NC	M2Ch04 RL	M2Ch11 L

SLOT 3

J7	J4	AD/DA	DA (J7)	RTD	Discrete	TTL	Signal	S/D	Differential
14	A20	M3Ch01 H	M3Ch01 H	M3Ch01 EX H	M3Ch01	M3Ch01	NC	Not Used	M3Ch01 H
34	A21	M3Ch01 L	M3Ch01 L	M3Ch01 EX L	M3Ch02	M3Ch02	NC	Not Used	M3Ch01 L
15	A22	M3Ch02 H	NC	M3Ch01 Sig H	M3Ch03	M3Ch03	NC	Not Used	M3Ch02 H
35	A23	M3Ch02 L	NC	M3Ch01 Sig L	M3Ch04	M3Ch04	NC	Not Used	M3Ch02 L
16	A24	M3Ch03 H	NC	M3Ch02 EX H	M3Vcc1-4	NC	NC	Not Used	M3Ch03 H
36	A25	M3Ch03 L	NC	M3Ch02 EX L	M3Gnd1-4	NC	NC	Not Used	M3Ch03 L
17	B20	M3Ch04 H	M3Ch02 H	M3Ch02 Sig H	M3Ch05	M3Ch05	M3Ch01	Not Used	M3Ch04 H
37	B21	M3Ch04 L	M3Ch02 L	M3Ch02 Sig L	M3Ch06	M3Ch06	GND	Not Used	M3Ch04 L
18	B22	M3Ch05 H	NC	M3Ch03 EX H	M3Ch07	M3Ch07	NC	Not Used	M3Ch05 H
38	B23	M3Ch05 L	NC	M3Ch03 EX L	M3Ch08	M3Ch08	NC	Not Used	M3Ch05 L
19	B24	AGND/NC	NC	M3Ch03 Sig H	M3Vcc5-8	NC	M3Ch02	Not Used	M3Ch06 H
39	B25	NC	NC	M3Ch03 Sig L	M3Gnd5-8	NC	GND	Not Used	M3Ch06 L
53	C20	M3Ch06 H	M3Ch03 H	M3Ch04 EX H	M3Ch09	M3Ch09	NC	Not Used	M3GND
73	C21	M3Ch06 L	M3Ch03 L	M3Ch04 EX L	M3Ch10	M3Ch10	NC	Not Used	M3GND
54	C22	M3Ch07 H	NC	M3Ch04 Sig H	M3Ch11	M3Ch11	M3Ch03	Not Used	M3Ch07 H
74	C23	M3Ch07 L	NC	M3Ch04 Sig L	M3Ch12	M3Ch12	GND	Not Used	M3Ch07 L
55	C24	M3Ch08 H	NC	M3Ch05 EX H	M3Vcc9-12	NC	NC	Not Used	M3Ch08 H
75	C25	M3Ch08 L	NC	M3Ch05 EX L	M3Gnd9-12	NC	NC	Not Used	M3Ch08 L
56	D20	M3Ch09 H	M3Ch04 H	M3Ch05 Sig H	M3Ch13	M3Ch13	M3Ch04	Not Used	M3Ch09 H
76	D21	M3Ch09 L	M3Ch04 L	M3Ch05 Sig L	M3Ch14	M3Ch14	GND	Not Used	M3Ch09 L
57	D22	M3Ch10 H	NC	M3Ch06 EX H	M3Ch15	M3Ch15	NC	Not Used	M3Ch10 H
77	D23	M3Ch10 L	NC	M3Ch06 EX L	M3Ch16	M3Ch16	NC	Not Used	M3Ch10 L
58	D24	NC	NC	M3Ch06 Sig H	M3Vcc13-16	NC	NC	Not Used	M3Ch11 H
78	D25	NC	NC	M3Ch06 Sig L	M3Gnd13-16	NC	NC	Not Used	M3Ch11 L

SLOT 4

J6	J5	AD/DA	DA (J7)	RTD	Discrete	TTL	Signal	S/D	Differential
1	A1	M4Ch01 H	M4Ch01 H	M4Ch01 EX H	M4Ch01	M4Ch01	NC	M4Ch01 S1	M4Ch01 H
21	A2	M4Ch01 L	M4Ch01 L	M4Ch01 EX L	M4Ch02	M4Ch02	NC	M4Ch01 S3	M4Ch01 L
2	A3	M4Ch02 H	NC	M4Ch01 Sig H	M4Ch03	M4Ch03	NC	M4Ch01 S2	M4Ch02 H
22	A4	M4Ch02 L	NC	M4Ch01 Sig L	M4Ch04	M4Ch04	NC	M4Ch01 S4	M4Ch02 L
3	A5	M4Ch03 H	NC	M4Ch02 EX H	M4Vcc1-4	NC	NC	M4Ch01 RH	M4Ch03 H
23	A6	M4Ch03 L	NC	M4Ch02 EX L	M4Gnd1-4	NC	NC	M4Ch01 RL	M4Ch03 L
4	B1	M4Ch04 H	M4Ch02 H	M4Ch02 Sig H	M4Ch05	M4Ch05	M4Ch01	M4Ch02 S1	M4Ch04 H
24	B2	M4Ch04 L	M4Ch02 L	M4Ch02 Sig L	M4Ch06	M4Ch06	GND	M4Ch02 S3	M4Ch04 L
5	B3	M4Ch05 H	NC	M4Ch03 EX H	M4Ch07	M4Ch07	NC	M4Ch02 S2	M4Ch05 H
25	B4	M4Ch05 L	NC	M4Ch03 EX L	M4Ch08	M4Ch08	NC	M4Ch02 S4	M4Ch05 L
6	B5	AGND/NC	NC	M4Ch03 Sig H	M4Vcc5-8	NC	M4Ch02	M4Ch02 RH	M4Ch06 H
26	B6	NC	NC	M4Ch03 Sig L	M4Gnd5-8	NC	GND	M4Ch02 RL	M4Ch06 L
40	C1	M4Ch06 H	M4Ch03 H	M4Ch04 EX H	M4Ch09	M4Ch09	NC	M4Ch03 S1	M4GND
60	C2	M4Ch06 L	M4Ch03 L	M4Ch04 EX L	M4Ch10	M4Ch10	NC	M4Ch03 S3	M4GND
41	C3	M4Ch07 H	NC	M4Ch04 Sig H	M4Ch11	M4Ch11	M4Ch03	M4Ch03 S2	M4Ch07 H
61	C4	M4Ch07 L	NC	M4Ch04 Sig L	M4Ch12	M4Ch12	GND	M4Ch03 S4	M4Ch07 L
42	C5	M4Ch08 H	NC	M4Ch05 EX H	M4Vcc9-12	NC	NC	M4Ch03 RH	M4Ch08 H
62	C6	M4Ch08 L	NC	M4Ch05 EX L	M4Gnd9-12	NC	NC	M4Ch03 RL	M4Ch08 L
43	D1	M4Ch09 H	M4Ch04 H	M4Ch05 Sig H	M4Ch13	M4Ch13	M4Ch04	M4Ch04 S1	M4Ch09 H
63	D2	M4Ch09 L	M4Ch04 L	M4Ch05 Sig L	M4Ch14	M4Ch14	GND	M4Ch04 S3	M4Ch09 L
44	D3	M4Ch10 H	NC	M4Ch06 EX H	M4Ch15	M4Ch15	NC	M4Ch04 S2	M4Ch10 H
64	D4	M4Ch10 L	NC	M4Ch06 EX L	M4Ch16	M4Ch16	NC	M4Ch04 S4	M4Ch10 L
45	D5	NC	NC	M4Ch06 Sig H	M4Vcc13-16	NC	NC	M4Ch04 RH	M4Ch11 H
65	D6	NC	NC	M4Ch06 Sig L	M4Gnd13-16	NC	NC	M4Ch04 RL	M4Ch11 L

SLOT 5

J6	J5	AD/DA	DA (J7)	RTD	Discrete	TTL	Signal	S/D	Differential
27	A9	M5Ch01 H	M5Ch01 H	M5Ch01 EX H	M5Ch01	M5Ch01	NC	M5Ch01 S1	M5Ch01 H
8	A10	M5Ch01 L	M5Ch01 L	M5Ch01 EX L	M5Ch02	M5Ch02	NC	M5Ch01 S3	M5Ch01 L
28	A11	M5Ch02 H	NC	M5Ch01 Sig H	M5Ch03	M5Ch03	NC	M5Ch01 S2	M5Ch02 H
9	A12	M5Ch02 L	NC	M5Ch01 Sig L	M5Ch04	M5Ch04	NC	M5Ch01 S4	M5Ch02 L
29	A13	M5Ch03 H	NC	M5Ch02 EX H	M5Vcc1-4	NC	NC	M5Ch01 RH	M5Ch03 H
10	A14	M5Ch03 L	NC	M5Ch02 EX L	M5Gnd1-4	NC	NC	M5Ch01 RL	M5Ch03 L
30	B9	M5Ch04 H	M5Ch02 H	M5Ch02 Sig H	M5Ch05	M5Ch05	M5Ch01	M5Ch02 S1	M5Ch04 H
11	B10	M5Ch04 L	M5Ch02 L	M5Ch02 Sig L	M5Ch06	M5Ch06	GND	M5Ch02 S3	M5Ch04 L
31	B11	M5Ch05 H	NC	M5Ch03 EX H	M5Ch07	M5Ch07	NC	M5Ch02 S2	M5Ch05 H
12	B12	M5Ch05 L	NC	M5Ch03 EX L	M5Ch08	M5Ch08	NC	M5Ch02 S4	M5Ch05 L
32	B13	AGND/NC	NC	M5Ch03 Sig H	M5Vcc5-8	NC	M5Ch02	M5Ch02 RH	M5Ch06 H
13	B14	NC	NC	M5Ch03 Sig L	M5Gnd5-8	NC	GND	M5Ch02 RL	M5Ch06 L
66	C9	M5Ch06 H	M5Ch03 H	M5Ch04 EX H	M5Ch09	M5Ch09	NC	M5Ch03 S1	M5GND
47	C10	M5Ch06 L	M5Ch03 L	M5Ch04 EX L	M5Ch10	M5Ch10	NC	M5Ch03 S3	M5GND
67	C11	M5Ch07 H	NC	M5Ch04 Sig H	M5Ch11	M5Ch11	M5Ch03	M5Ch03 S2	M5Ch07 H
48	C12	M5Ch07 L	NC	M5Ch04 Sig L	M5Ch12	M5Ch12	GND	M5Ch03 S4	M5Ch07 L
68	C13	M5Ch08 H	NC	M5Ch05 EX H	M5Vcc9-12	NC	NC	M5Ch03 RH	M5Ch08 H
49	C14	M5Ch08 L	NC	M5Ch05 EX L	M5Gnd9-12	NC	NC	M5Ch03 RL	M5Ch08 L
69	D9	M5Ch09 H	M5Ch04 H	M5Ch05 Sig H	M5Ch13	M5Ch13	M5Ch04	M5Ch04 S1	M5Ch09 H
50	D10	M5Ch09 L	M5Ch04 L	M5Ch05 Sig L	M5Ch14	M5Ch14	GND	M5Ch04 S3	M5Ch09 L
70	D11	M5Ch10 H	NC	M5Ch06 EX H	M5Ch15	M5Ch15	NC	M5Ch04 S2	M5Ch10 H
51	D12	M5Ch10 L	NC	M5Ch06 EX L	M5Ch16	M5Ch16	NC	M5Ch04 S4	M5Ch10 L
71	D13	NC	NC	M5Ch06 Sig H	M5Vcc13-16	NC	NC	M5Ch04 RH	M5Ch11 H
52	D14	NC	NC	M5Ch06 Sig L	M5Gnd13-16	NC	NC	M5Ch04 RL	M5Ch11 L

SLOT 6

J6	J5	AD/DA	DA (J7)	RTD	Discrete	TTL	Signal	S/D	Differential
14	A17	M6Ch01 H	M6Ch01 H	M6Ch01 EX H	M6Ch01	M6Ch01	NC	Not Used	M6Ch01 H
34	A18	M6Ch01 L	M6Ch01 L	M6Ch01 EX L	M6Ch02	M6Ch02	NC	Not Used	M6Ch01 L
15	A19	M6Ch02 H	NC	M6Ch01 Sig H	M6Ch03	M6Ch03	NC	Not Used	M6Ch02 H
35	A20	M6Ch02 L	NC	M6Ch01 Sig L	M6Ch04	M6Ch04	NC	Not Used	M6Ch02 L
16	A21	M6Ch03 H	NC	M6Ch02 EX H	M6Vcc1-4	NC	NC	Not Used	M6Ch03 H
36	A22	M6Ch03 L	NC	M6Ch02 EX L	M6Gnd1-4	NC	NC	Not Used	M6Ch03 L
17	B17	M6Ch04 H	M6Ch02 H	M6Ch02 Sig H	M6Ch05	M6Ch05	M6Ch01	Not Used	M6Ch04 H
37	B18	M6Ch04 L	M6Ch02 L	M6Ch02 Sig L	M6Ch06	M6Ch06	GND	Not Used	M6Ch04 L
18	B19	M6Ch05 H	NC	M6Ch03 EX H	M6Ch07	M6Ch07	NC	Not Used	M6Ch05 H
38	B20	M6Ch05 L	NC	M6Ch03 EX L	M6Ch08	M6Ch08	NC	Not Used	M6Ch05 L
19	B21	AGND/NC	NC	M6Ch03 Sig H	M6Vcc5-8	NC	M6Ch02	Not Used	M6Ch06 H
39	B22	NC	NC	M6Ch03 Sig L	M6Gnd5-8	NC	GND	Not Used	M6Ch06 L
53	C17	M6Ch06 H	M6Ch03 H	M6Ch04 EX H	M6Ch09	M6Ch09	NC	Not Used	M6GND
73	C18	M6Ch06 L	M6Ch03 L	M6Ch04 EX L	M6Ch10	M6Ch10	NC	Not Used	M6GND
54	C19	M6Ch07 H	NC	M6Ch04 Sig H	M6Ch11	M6Ch11	M6Ch03	Not Used	M6Ch07 H
74	C20	M6Ch07 L	NC	M6Ch04 Sig L	M6Ch12	M6Ch12	GND	Not Used	M6Ch07 L
55	C21	M6Ch08 H	NC	M6Ch05 EX H	M6Vcc9-12	NC	NC	Not Used	M6Ch08 H
75	C22	M6Ch08 L	NC	M6Ch05 EX L	M6Gnd9-12	NC	NC	Not Used	M6Ch08 L
56	D17	M6Ch09 H	M6Ch04 H	M6Ch05 Sig H	M6Ch13	M6Ch13	M6Ch04	Not Used	M6Ch09 H
76	D18	M6Ch09 L	M6Ch04 L	M6Ch05 Sig L	M6Ch14	M6Ch14	GND	Not Used	M6Ch09 L
57	D19	M6Ch10 H	NC	M6Ch06 EX H	M6Ch15	M6Ch15	NC	Not Used	M6Ch10 H
77	D20	M6Ch10 L	NC	M6Ch06 EX L	M6Ch16	M6Ch16	NC	Not Used	M6Ch10 L
58	D21	NC	NC	M6Ch06 Sig H	M6Vcc13-16	NC	NC	Not Used	M6Ch11 H
78	D22	NC	NC	M6Ch06 Sig L	M6Gnd13-16	NC	NC	Not Used	M6Ch11 L

NOTE 1: Contact Factory

AGND/NC is AGND for A/D Module, and NO CONNECT for D/A Module.

ALL D/A Low signals (MxChxx Sig L) are connected to AGND, Common within that module, isolated from all other modules and isolated from the cPCI bus.

For DISCRETE Modules, where n=1 to 6, MnGnd1-4, MnGnd5-8, MnGnd9-12 and McGnd13-16 are all common for that module. However, each pin should be individually wired for optimal power current distribution throughout that module. MnGnd and MnVcc MUST be wired for proper operation.

Encoder/Commutation Output Connection

Rear J3 and J4 Connector

J3	Ch.	J3	Ch.	J3	Ch.	J3	Ch.	J4	Ch.
A1	AHI-CH1	E5	AHI-CH5	B10	AHI-CH9	C15	AHI-CH13	E1	IDXHI-CH16
B1	ALO-CH1	E6	ALO-CH5	A10	ALO-CH9	D15	ALO-CH13	E2	IDXLO-CH16
C1	BHI-CH1	D6	BHI-CH5	A11	BHI-CH9	E15	BHI-CH13		
D1	BLO-CH1	C6	BLO-CH5	B11	BLO-CH9	E16	BLO-CH13		
E1	IDXHI-CH1	B6	IDXHI-CH5	C11	IDXHI-CH9	D16	IDXHI-CH13		
E2	IDXLO-CH1	A6	IDXLO-CH5	D11	IDXLO-CH9	C16	IDXLO-CH13		
D2	AHI-CH2	A7	AHI-CH6	E11	AHI-CH10	B16	AHI-CH14		
C2	ALO-CH2	B7	ALO-CH6	E12	ALO-CH10	A16	ALO-CH14		
B2	BHI-CH2	C7	BHI-CH6	D12	BHI-CH10	A17	BHI-CH14		
A2	BLO-CH2	D7	BLO-CH6	C12	BLO-CH10	B17	BLO-CH14		
A3	IDXHI-CH2	E7	IDXHI-CH6	B12	IDXHI-CH10	C17	IDXHI-CH14		
B3	IDXLO-CH2	E8	IDXLO-CH6	A12	IDXLO-CH10	D17	IDXLO-CH14		
C3	AHI-CH3	D8	AHI-CH7	A13	AHI-CH11	E17	AHI-CH15		
D3	ALO-CH3	C8	ALO-CH7	B13	ALO-CH11	E18	ALO-CH15		
E3	BHI-CH3	B8	BHI-CH7	C13	BHI-CH11	D18	BHI-CH15		
E4	BLO-CH3	A8	BLO-CH7	D13	BLO-CH11	C18	BLO-CH15		
D4	IDXHI-CH3	A9	IDXHI-CH7	E13	IDXHI-CH11	B18	IDXHI-CH15		
C4	IDXLO-CH3	B9	IDXLO-CH7	E14	IDXLO-CH11	A18	IDXLO-CH15		
B4	AHI-CH4	C9	AHI-CH8	D14	AHI-CH12	A19	AHI-CH16		
A4	ALO-CH4	D9	ALO-CH8	C14	ALO-CH12	B19	ALO-CH16		
A5	BHI-CH4	E9	BHI-CH8	B14	BHI-CH12	C19	BHI-CH16		
B5	BLO-CH4	E10	BLO-CH8	A14	BLO-CH12	D19	BLO-CH16		
C5	IDXHI-CH4	D10	IDXHI-CH8	A15	IDXHI-CH12				
D5	IDXLO-CH4	C10	IDXLO-CH8	B15	IDXLO-CH12				

NOTE: For commutation (A,B,C) outputs: A Hi becomes A, B Hi becomes B, and Index Hi becomes C.

PART NUMBER DESIGNATION

78C1 – XX XX XX XX XX XX X X X

Slot # 1 2 3 4 5 6

MODULE (SLOT) DEFINITION

Enter Modules "A through Y" [1] for each of Slots 1 through 6; "Z0" if slot not used

A/D (Module C1)	Ten (10) A/D (1.25 VDC to 10.0 VDC FS) Uni or bipolar
A/D (Module C2)	Ten (10) A/D (40VDC) Uni or bipolar
A/D (Module C3)	Ten (10) 4 – 20ma Current Measurement Module
A/D (Module C4)	Ten (10) A/D (50VDC) Uni or bipolar
Signal (Module E1)	Four (4) Programmable Function Generators
D/A (Module F1)	Ten (10) D/A Outputs ±10 VDC, cPCI ISOLATED
D/A (Module F3)	Ten (10) D/A Outputs ±5 VDC, cPCI ISOLATED
D/A (Module J3)	Ten (10) D/A Outputs ±1.25 VDC, cPCI ISOLATED
D/A (Module J5)	Ten (10) D/A Outputs ±2.5 VDC, cPCI ISOLATED
D/A (Module J7)	Four (4) D/A Outputs ±20 to ±80 VDC, cPCI ISOLATED
I/O (Module D1)	Sixteen (16) TTL (0-5V), Programmable for Input or Output
I/O (Module D2)	Eleven (11) Differential Multi-Mode Transceivers
I/O (Module K2)	Sixteen (16) Discrete (0-40V), ISOLATED, Programmable for Input or Output
I/O (Module K4)	Sixteen (16) Discrete (0-40V), NON-ISOLATED, Programmable for Input or Output
RTD (Module G1)	Six (6) four-wire Platinum RTD
R/D (Module R2)	Four (4) 400Hz 11.8V_{RMS}, 11.8V_{L-L} Resolver Measurement[1]
R/D (Module R3)	Four (4) 400Hz Auto ranging Resolver Measurement[1]
R/D (Module R4)	Four (4) 1200Hz 26V_{RMS}, 11.8V_{L-L} Resolver Measurement[1]
S/D (Module S1)	Four (4) 400Hz Synchro Measurement[1]
S/D (Module S2)	Four (4) 60-400Hz Synchro Measurement[1]

ON-BOARD REFERENCE MODULE

USE FOR S/D OR R/D APPLICATIONS ONLY
0 = No On-Board Reference Module
1 = 2-28Vrms, 360-10kHz Programmable On-Board Reference Module
2 = Not Used
3 = 115Vrms Fixed, 360-10kHz Programmable On-Board Reference Module

MECHANICAL

F = Front Panel (J6 & J7) I/O only.
P = Rear (J1, J4, & J5) I/O only
W= P with Wedgelocks
B = Front Panel (J6 & J7) and Rear (J1, J4, & J5) I/O.

ENVIRONMENTAL

C = 0 TO 70
E = -40 TO +85
H = E WITH REMOVABLE COATING
K = C WITH REMOVABLE COATING

Note: 1. For these functions and other frequency ranges, see 64CS3 or 64SD3 and/or contact factory.

REVISION PAGE

Revision	Description of Change	Engineer	Date
1.2	Adds Front Panel Pin-out and adds PN Mechanical Option B	GS	12/22/03
1.3	Current with 64C1 rev 3.4 Module specifications	GS	1/9/4
1.4	AD module Range and Polarity descriptions details all polarity ranges.	GS	2/4/4
1.5	Adds Rear Panel connector pin-outs. Adds Reference Output Pins.	GS	2/27/4
1.6	Module K2 Vcc >=8 Volts. Output is 8 to 40Vdc. J7 supports slots 1-3.	GS	3/3/4
1.7	Adds reference Rhi and Rlo OUT for front AND rear panel connectors. Signal module E1 Power +5 VDC at 0.6A per module	GS	3/18/4
1.8	Changed nomenclature from D/A "Range" to "Polarity" register. COMMERCIAL AND MILITARY TEMP RANGE. Amends Back Panel Connector J5 Pin-out.	GS	4/12/4
1.9	Removed unimplemented control pins J7.20 & J7.59 and J6.20 & J6.59 and edited J3 & J4 encoder pin-out channels 12 through 16.	GS	4/19/4
2.0	All cPCI Memory Maps are indexed by 4 (not 2). Adds Interrupt Status and Clear registers.	GS	6/8/4
2.1	Spec is no longer preliminary. Rear Panel Reference output pins are TBD. Added Encoder output BIT map. Conducted cooled versions available	GS	7/8/4
2.2	User provided Vcc must be greater than or equal to any input signal or current limited to 10ma.	GS	8/5/4
2.3	Appends AD spec where range is ±FS or 0 to FS VDC.	GS	8/12/4
2.4	Adds Commutation Programming to S module	GS	8/18/4
2.5	Adds Ref Hi and Lo OUT to Rear Panel Connector	GS	8/24/4
2.6	Adds TOC. Module D1, 0x0A4 Input/Output Format is for Ch.01-8 (not 1-16).	GS	10/18/4
2.7	A/D is sampled at 50 I (not type 50 i). Corrects Product Memory Map Configuration, i.e. each module starts at 000, 200, 400, 600, 800 or A00	GS	10/27/4
2.8	D1 Power requirement is 40mA on 5V supply. D1 is TTL 5V System Logic Supply. J5 is ±2.5 VDC. Adds F3 ±.5 VDC D/A module. E1 programming is accurate to spec at a programmed frequency of more than or equal to 10 Hz. E1 output regulation is 7%. Updates DA J7 Output Range programming, LSB is 10v. J7 Bit tests to 2% accuracy.	GS	11/15/4
2.9	Adds Module R2, R3, and R4. J7 is 10ma max / channel, up to 80V output. Current reduced up to 90VDC. Reference module is for SD or RD applications only.	GS	¼/5
3.0	When phase locked, phase is reset when channel 1 frequency is changed. If phase is NOT locked, phase remains unchanged when frequency is changed. AD module C1 is over-voltage protected to 12v continuous.	GS	1/25/5
3.1	Module J3, J5, F1, F3 and J7 are cPCI ISOLATED. J7 output is 20-80v, BIT is to 2% accur. G1 interfaces with any RTD up to 2000 ohm range.	GS	2/14/8
3.2	K3 output is +0 VDC to +40 VDC. Output logic is defined by the user provided Vcc voltage (≥ 8 volts) to that channel bank. There are four channels per bank.	GS	3/2/5
3.3	All D modules debounce LSB is 1.28 microseconds.	GS	3/29/5
3.4	Module C3 input voltage: Not to exceed ±3 volts.	GS	3/31/5
3.5	Range and Polarity to C1 module programs up to 10 volt range	GS	4/11/5
3.6	Update AD power requirements. As of 4/5/05, +5V is 500ma typ, 750ma max, no ±12V For 5V Discrete I/O applications use D1. Adds Module Special Spec, DSP & FPGA registers.	GS	4/20/5
3.7	Replaces Module Special Spec with Module Design Revision. Adds Module Design Version	GS	5/10/5
3.8	J7 range is 20-80	GS	5/17/5
3.9	Updates Module Memory Map registers index	GS	6/2/5
4.0	Module D2 Read I/O corresponds to 11 channels	GS	6/20/5
4.1	New Address	KL	04/25/07