Model PCI-76C2 (Half-Size)

A/D, D/A, Discrete I/O, TTL I/O, RTD, Synchro/Resolver and LVDT/RVDT Channels

PCI bus

MULTI-FUNCTION CARD

A/D, D/A, Discrete I/O, TTL I/O, RTD, Synchro / Resolver and LVDT/RVDT Channels

EXTENSIVE (Built-In) DIAGNOSTICS

Card Photo - (Typical Configuration / Heatsink not shown for clarity)

FEATURES

- Multiple functions on a single slot, half size PCI card
- No damage if Signals are applied when card is not powered
- Software Driver/Library and Support Kit available at http://www.naii.com

DESCRIPTION

This universal card eliminates the need for specialized, single function cards by providing an assortment of functions on one single card. The "mother board" contains 3 **independent module slots**, each of which can be populated with a function specific module. The available functions are as follows:

Function	Module	Channels	Details
A/D	C1, C2, C4, C3	10	±1.25 to ±50 VDC and 4-20ma versions
D/A	J3, J5, F3, F1	10	±1.25, ±2.5, ±5V, ±10 VDC, Isolated or Non-Isolated versions
	J7	4	High Voltage, ±20 to ±80 VDC, Isolated
	F5	4	High Current, ±20 VDC at 100 mA max, Isolated
Digital I/O	D7	16	TTL (5V System Logic Supply), Programmable for Input or Output
	D8	11	Differential Multi-Mode Transceivers
Signal Generator	E5	4	Function Generator, 10-130kHz, 0-15Vpp (5.3 Vrms)
RTD	G4	6	3 or 4 wire Platinum Resistance Temperature Device Measurement
Discrete I/O	K6	16	Discrete (0-80 VDC), Programmable for Input or Output, Isolated
L(R)VDT/D[1]	L*	4	L(R)VDT-to-Digital, 2, 3 or 4 wire L(R)VDT
S(R)/D[1]	S*	4	Synchro (or Resolver)-to-Digital Measurement
Reference	W1	1	2.2 VA programmable. 2-115 Vrms, 50 Hz-10 KHz

Notes:

1: For these functions and other frequency ranges, see 76CS1 and/or contact factory.

* Indicates wide selection (see part number selection)

Automatic background BIT testing, an important feature is always enabled and continually checks the health of each channel. There is no need to guess or make assumptions about system performance. A fault is immediately reported and the specific channel is identified. This capability is of tremendous benefit because it identifies and reports a failure, without the need to shut down the equipment for troubleshooting. Testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card and can be disabled on a per channel basis. (See Operational Instructions for further detail within this specification.)

TABLE OF CONTENTS

SPECIFICATIONS

General	**For the Carrier Card (Mother Board)**
Signal Logic Level:	Supports 5V PCI bus.
Power (Mother board):	TBD, then add power for each individual module.
Temperature, operating:	"C" =0°C to +70°C, "E" =-40°C to +85°C (see part number)
Storage temperature:	-55°C to +105°C
Size:	Half-Size PCI (short card) @ 6.6" x 4.2" or 16.78cm x 10.67cm
Weight:	TBD oz. (TBDg) unpopulated. add weight for each module (typically 1 oz. each)

A/D (Module C1)	**Ten (10) A/D (1.25 VDC to 10.0 VDC FS) Uni or bipolar**
Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as F.S. inputs of: 10.00, 5.00, 2.50, or 1.25 volts where range is ±FS or 0 to FS VDC. The ability to set lower voltages for Full Scale, assures the utilization of the full resolution.
Over-voltage.	No damage up to ±12 V continuous; ±30 V momentary
Open Input sense:	This module will sense and report unconnected Inputs
Input Impedance:	1 MΩ min.
Accuracy:	0.05 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB's max. over temperature
Sampling rate:	200 KHz per channel
Band Width:	20 KHz
Group delay:	30 microseconds (time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz
Common mode voltage:	Signal voltage plus Common mode equals 10.5 volts
Output Logic:	Bipolar output in two's complement. 7FFF is max. positive, 8000 is max. negative. Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns.
Power:	500ma typical, 750ma max.
Weight:	1 oz. (28g)

Note: A/D differential inputs must not "float" (i.e. common mode voltage as referenced to PCI system ground must not exceed maximum specifications for the module).

A/D (Module C2)	**Ten (10) A/D (40VDC) Uni or bipolar**
Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as full scale inputs of: 40.00, 20.00, 10.00, or 5.00 volts where range is ±FS or 0 to FS VDC. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution. This module will not sense open Inputs
Over-voltage protected:	±100 Volts
Input Impedance:	500 kΩ min. (Differential)
Accuracy:	0.1 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB's max. over temperature
Sampling rate:	200 KHz per channel
Band width:	20 KHz per channel
Group delay:	30 microseconds (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz
Output Logic:	Bipolar output in two's complement. 7FFF is max. positive, 8000 is max. negative. Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	500ma typical, 750ma max.
Weight:	1 oz. (28g)

Note: A/D differential inputs must not "float" (i.e. common mode voltage as referenced to PCI system ground must not exceed maximum specifications for the module).

A/D (Module C3)	**Ten (10) 4-20ma Current Measurement Module**
Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input, 0-25ma)
Input scaling:	Ten (10) unipolar channels, 0-25ma full scale. This module will not sense open Inputs
Input voltage:	Not to exceed ±3 volts.
Input Impedance:	100 Ω min.
Accuracy:	0.1 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±8 LSB's max. over temperature
Sampling rate:	200 KHz per channel
Band width:	20 KHz per channel
Group delay:	30 microseconds (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 l in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 l
Common mode voltage:	Signal voltage plus Common mode equals 80 volts
Output Logic:	Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	500ma typical, 750ma max.
Weight:	1 oz. (28g)

Note: A/D differential inputs must not "float" (i.e. common mode voltage as referenced to PCI system ground must not exceed maximum specifications for the module).

A/D (Module C4)	**Ten (10) A/D (50VDC) Uni or bipolar**
Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as full scale inputs of: 50.00, 25.00, 12.50, or 6.25 volts where range is ±FS or 0 to FS VDC. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution. This module will not sense open Inputs
Over-voltage protected:	±100 Volts
Input Impedance:	500 kΩ min. (Differential)
Accuracy:	0.1 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB's max. over temperature
Sampling rate:	200 KHz per channel
Band width:	20 KHz per channel
Group delay:	30 microseconds (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 I in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 I
Common mode voltage:	Signal voltage plus Common mode equals 80 volts
Output Logic:	Bipolar output in two's complement. 7FFF is max. positive, 8000 is max. negative. Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	500ma typical, 750ma max.
Weight:	1 oz. (28g)

Note: A/D differential inputs must not "float" (i.e. common mode voltage as referenced to PCI system ground must not exceed maximum specifications for the module).

I/O (Module D7)	**Sixteen (16) TTL, Programmable for Input or Output**
TTL Input	
Input levels:	TTL and CMOS compatible, single ended inputs Each channel incorporates a 100 KΩ pull-down resistor $V_{in\ L:}$ 0.8 V = "0" $V_{in\ H:}$ 2.0 V = "1" $V_{in\ max.:}$ 5.0 V I_{IN} = ± 50μA
Read Delay:	1.02 μseconds
De-bounce:	Programmable per bit from 0 to 255 microseconds. LSB= 1 microsecond.
TTL Output	
Output levels:	TTL/CMOS, single ended outputs
Drive Capability:	$V_{out\ L:}$ +0.5 V max. sink 32 mA max. $V_{out\ H:}$ 3.8 V min. source -32 mA max.
Output current:	Channel will withstand a current of 50ma for 4 microseconds and will then be turned off.
Rise/Fall time:	10 ns into a 50pf load
Write Delay:	1.02 μseconds
Power:	+5 VDC System Logic Supply, at 40mA per module
Weight:	1 oz. (28g)

I/O (Module D8)	**Eleven (11) Differential Multi-Mode Transceivers**	
Mode of Operation:	422 (Differential)	485 (Differential)
Input		
Receiver Input Levels:	-10V to +10V	-7V to +12V
Receiver Input Resistance:	120Ω	>12kΩ
Receiver Input Sensitivity:	±200mV	±200mV
	(Each channel incorporates a 120 Ω termination resistor that can be programmed on a channel by channel basis)	
Read Delay:	1.02 μseconds	
Filtering	1-128, μseconds programmable	
Output		
Driver Output Voltage:	-0.25V to +6V max.	-0.25V to +6V max.
Driver Output Signal Level (Loaded minimum)	±2V	±1.5V
Driver Output Signal Level (Unloaded maximum)	±6V	±6V
Driver Load Impedance:	100Ω	54Ω
Max. Driver Current in Hi Z State (Power ON):	N/A	±100μA
Max. Driver Current in Hi Z State (Power OFF):	±100μA	±100μA
Write Delay:	1.02 μseconds	
Protection:	Short circuit protected, Thermal shutdown, Built-in current limiting	
Rise/Fall time:	31 ns into a 50pf load	
Power (Per 11 channel module):	+5VDC at 1Watt quiescent, 1.8Watts fully loaded (54Ω load per channel)	
Weight:	1 oz. (28g)	

Signal (Module E5)	**Four (4) Programmable Frequency Generators**
Output Signal:	Sine, Triangular, or Square Wave, one per channel
Output Frequency:	10 – 130kHz with 1Hz resolution
Output Voltage:	0 – 10Volts peak (7.07Vrms), Programmable, per channel
Accuracy	± 6% FS volts, for frequencies <100Hz
	± 1% FS volts, 100Hz – 20kHz
	± 6% FS volts, for frequencies >20kHz
Load:	600 ohms min.
Regulation:	7% max. No load to full load.
Phase:	0 – 359.912 ±1% with 0.088° resolution, relative to channel 1. Default is 0.
Power:	+5 VDC at 0.6A per module
Weight:	1 oz. (28g)

D/A (Module F1)	**Ten (10) D/A Outputs ±10 VDC, PCI ISOLATED**
Output range:	±10 VDC or 0 to 10 VDC, programmable. For other ranges contact customer service. Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Non-linearity:	0.01% FS over temperature
Gain error:	0.02% over temperature
Output format:	Optically isolated in groups of ten (250 V to PCI power)
Settling time:	10 μs typ. (15 μs max.)
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	5 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g)

D/A (Module F3)	**Ten (10) D/A Outputs ±5 VDC, PCI GND ISOLATED**
Output range:	±5 VDC or 0 to 5 VDC, programmable. For other ranges contact customer service. Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Non-linearity:	0.01% FS over temperature
Gain error:	0.02% over temperature
Output format:	Optically isolated in groups of ten (250 V to PCI power)
Settling time:	10 μs max
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	5 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g)

D/A (Module F5)	**Four (4) D/A Outputs ±20VDC at 100 mA, isolated from PCI GND**
Output range:	±20 VDC or 0 to 20 VDC, programmable. Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Non-linearity:	0.01% FS over temperature
Gain error:	0.02% over temperature
Output format:	Optically isolated in groups of ten (250 V to PCI power)
Settling time:	10 μs max
Load:	100 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. Short circuit protected. When current exceeds 110 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	5 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g)

RTD (Module G4)	**Six (6) four-wire Platinum RTD**
Resolution:	16 bits
RTD Interface:	Interfaces with 100Ω and 500Ω RTDs, or any RTD whose operating resistance is up to 2000Ω under the required operating conditions.
Open Input sense:	This module will sense unconnected Inputs. Only one open wire out of four will set flag
Excitation:	1 milliamp/channel
Accuracy:	0.8Ω for 2kΩ range, over temperature and with a 3.75 Hz bandwidth 0.27Ω for 655Ω range, over temperature and with a 3.75 Hz bandwidth
Grounds:	Each input has a separate return, but all are common and connected to PCI ground.
Update rate:	Each channel is updated seven times per second
Output Format:	Resistance
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns.
Power:	+ 12 VDC at 25 ma typical 50 ma max. +5 VDC at 320 ma typical, 500 ma max
Weight:	1 oz.

D/A (Module J3):	**Ten (10) D/A Outputs ±1.25 VDC, PCI GND ISOLATED**
Output range:	±1.25 VDC or 0 to +1.25 VDC, programmable. For other ranges contact factory Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Output format:	Optically isolated in groups of ten (250 V to PCI power)
Settling time:	10 μs max.
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. 5 KΩ min. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	5 microseconds/channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns.
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max.
Weight:	1 oz. (28g)

D/A (Module J5)	**Ten (10) D/A Outputs ±2.5 VDC, PCI GND ISOLATED**
Output range:	±2.5 VDC or 0 to +2.5 VDC, programmable. For other ranges contact factory Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Output format:	Optically isolated in groups of ten (250 V to PCI power)
Settling time:	350 μs max
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. 5 KΩ min. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	5 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g)

D/A (Module J7)	**Four (4) D/A Outputs ±20 to ±80 VDC, PCI ISOLATED**
Output range:	±20 to ±80 VDC. Output is set to 0 at reset or Power-on, Programmable in pairs, from ±20V to ±80V.
Returns:	Each D/A return has separate pins that are common within each module. These returns are isolated from PCI ground
Resolution:	12 bits/channel
Accuracy:	0.15% FS
Settling time:	10 μs
Load:	10 ma/channel max.(Source or Sink). Up to 80VDC. Output current reduced up to 90VDC. Short circuit protected.
Output impedance:	<1 Ω
Update rate:	10 microseconds per channel
Output control:	via software Enable/Disable of DC/DC converter.
Power:	+5 VDC, 250ma max per module
Weight:	1 oz. (28g)

Discrete (Module K6) **SIXTEEN (16) Channels; 0 to 80 volt discrete, (isolated from PCI ground), Programmable for Input or Output. Redundant safe.**

INPUT CHARACTERISTICS:

Input range:	0 to +80 VDC for level sensing. For contact sensing, Vcc per channel bank, must be between 3 VDC min. and 80 VDC max. There are 4 channels per bank.
Voltage/Contact Sensing:	Software selectable per bit. Input is self-contained and requires no Vcc. However, if Input is used as a current source to detect switch closures, Vcc will be required.
Input Pulse Detection:	A pulse, of 5µs min. width, will be sensed and indicated by the appropriate Hi–Lo or Lo-Hi Transition Interrupt
Input Impedance:	105kΩ (with or without power applied to module)
Switching Threshold:	Four levels are programmable from 0 to 80 VDC with 10-bit resolution (0.98% FS) On, Off. Short to +V, Short to ground.
Accuracy of Set Point:	The greater of 5% signal value or 0.25 volts
ON/OFF Differential	0.25 V minimum recommended
De-bounce:	Programmable per bit from 0 to 0.655 seconds. LSB= 5 microseconds).
Update Rate:	Each channel is updated every 5 microseconds
Over-Voltage Protection:	100 VDC max.
Ground:	Four Ground pins per module (one for each group of 4 channels). All Grounds are common, but are isolated from PCI ground.
Protective circuits:	New protective circuits are incorporated that avoid damage should an Input Signal be applied when/if Vcc is missing.

OUTPUT CHARACTERISTICS:

Output Range:	0 to +80 VDC Output logic is defined by the user provided Vcc voltage to that channel bank. There are four banks with four channels per bank.
Ground	Four Ground pins per module (one for each group of 4 channels). All Grounds are common, but are isolated from PCI ground.
Output Current:	0.5 A max. per channel Short circuit protected. **Total current per module not to exceed 8 A.** Channel will withstand a current of 0.75A for 20ms and will then be turned off.
Output Load:	Directly drive inductive loads (relays); Reverse current protection diode is incorporated.
Output impedance:	0.12 ohms
Output Format:	Low-side switched, high-side switched or push-pull. Programmable per bit
Write Delay:	5 µs
Update Rate:	Each channel is updated every 20 microseconds
Over-Voltage Protection:	100 VDC max.
Thermal protection	is provided
Isolation:	Vcc-to-PCI Ground: 500 volts Module-to-PCI Power: 500 volts I/O Signal: 500 volts, Digital I/O is opto-isolated from PCI bus

Redundant applications:	**Two outputs can be connected in parallel (only *one* output set *on*). The output that is turned off will not pull down the signal of the active output.**
Isolation:	Vcc-to-PCI Ground: 500 volts Module-to-PCI Power: 500 volts I/O Signal: 500 volts, Digital I/O is opto-isolated from PCI bus
Power:	+5VDC at 100 mA. For contact sensing add (Vcc x Iset) x4 per bank of 4
Weight:	0.55 oz. (25gms)
Ground	4 Ground pins per module. All Grounds are common, but isolated from PCI ground.

LVDT (Module L*) See P/N Four (4) 3 or 4-wire measurements

Resolution:	16-bit
Accuracy:	0.025% FS
Bandwidth:	Default factory setting is 10% of excitation to 100 Hz max. However, BW is field programmable on a per channel basis. User has to program all parameters for each boot up or parameter will bet set to the default value.
Input format:	LVDT or RVDT
Input voltage:	Auto ranging from 2.0 to 28 Vrms.
Excitation voltage:	Not required for computation of output but should be connected to allow card to check for excitation loss.
Input Impedance:	60 kΩ
Frequency:	Specify between 360 Hz to 20 kHz, (See Part Number)
Phase shift:	Automatically compensates for phase shifts between the transducer excitation and Output up to ±60° (3-wire units ignore phase shift)
Wrap around Self Test:	Three powerful test methods are described in the Programming Instructions.
Power:	+ 5 VDC: 2mA
Weight:	1 oz. (28g)

S/D (Module S*) See P/N Four (4) Synchro/Resolver Measurement

This new generation offers additional programmability. Any channel is programmable for either Synchro or Resolver. The Band width will default to a factory set value (generally 10% of reference frequency) but will be field programmable. User has to program all parameters for each boot up or parameter will bet set to the default value.

Resolution:	16 bits (up to 24 bits for two-speed configuration)
Accuracy:	±1 arc-minute for single speed inputs ±1 arc-minute divided by the gear ratio for two-speed inputs
Tracking Rate:	150 RPS (Referred to the Fine input for two-speed configuration)
Bandwidth:	Default set at factory but per channel field programmable.
Input format:	Synchro/Resolver programmable. Default will be Synchro
Input voltage:	See P/N
Input Impedance:	60 kΩ min. at 26V_{L-L}; 260 kΩ min. at 90V_{L-L}
Reference Input:	See P/N.
Reference Zin	100 kΩ min.
Frequency Input:	50 Hz to 20 KHz (See part number)
Angle change alert:	Each channel can be set to a different angle differential. When that differential is exceeded, an interrupt (if enabled) is triggered. Default: “Ch. Disabled”. MSB=180°; Min. differential is 0.05°. Max differential that can be programmed is 179.9°.
Phase shift:	The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°.
Velocity, Digital:	16-bit resolution; Linearity: 0.1%. Scalable to 0.1°/sec resolution.
Wrap around Self Test:	The three different powerful test methods are detailed in the Description section and further described in the Programming Instructions.
Power:	+ 5 VDC: 2mA at 26V_{L-L}; 6mA at 90V_{L-L}
Weight:	1 oz. (28g)

Reference (Module W1)

	See P/N
Voltage:	2.0-115 Vrms programmable, resolution 0.1Vrms
Accuracy:	±2%
Frequency:	47Hz to 10kHz ±1% with 1Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	2.2 VA max. @ 40° min. inductive; 78mA @ 2-26VAC or 19mA @ 115VAC Note: Power is reduced linearly as the Reference Voltage is reduced.
Power Dissipation:	1A @ 5VA Load (3A peak)
Weight:	2 oz. (28g)

ADDRESS CONFIGURATION

This section provides programmers the information needed for developing drivers other than those supplied.

The following information resides in the PCI configuration registers:

Device ID	= 7692	(hex)
Vendor ID	= 15AC	(hex)
Rev	= 01	(hex)
Subsystem ID	= 000115AC	(hex)

Base Address = Assigned by the PCI BIOS. Interrogate the PCI BIOS for this information.

Required Address space = 32K for each card.

PRODUCT CONFIGURATION AND MEMORY MAP

This design provides multiple functions on a single slot, half size PCI card. When ordering, the customer selects an assortment of up to 3 modules to populate this 6-slot "mother board." The memory map follows the order of modules specified in the part number.

To address the register of any module, use the *Base* address to the entire card, add the *Module Offset* depending upon its slot (000, 800,…or 1000), and then add the *Register Offset* of interest (see module memory map.) The memory map of each selected module counts from, or is superimposed over its respective module offset. Thus, **Address = Base + Module Offset + Register Offset**.

For example, if a Digital I/O module were selected to populate module 1 and a Discrete I/O module were selected to populate module 2:

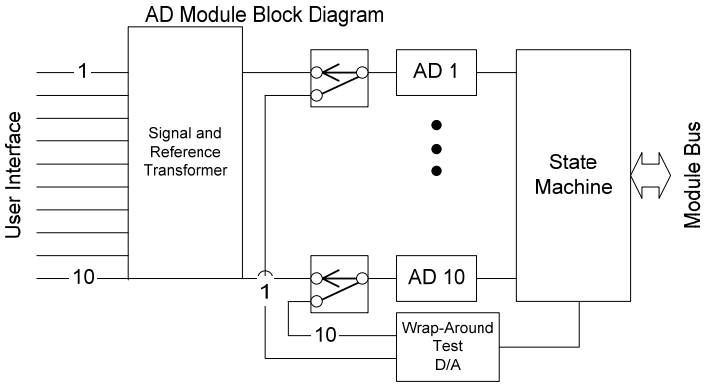
Address = Base + Module 1 Offset 000 + Digital I/O register 010 = Base + 010 hex
Address = Base + Module 2 Offset 800 + Discrete I/O register 024 = Base + 824 hex.

MEMORY MAP

0000	Module 1 Register…	0800	Module 2 Register…	1000	Module 3 Register…
0004		0804		1004	
0008		0808		1008	
000C		080C		100C	
0010	Module 1	0810	Module 2	1010	Module 3
.	Offset 000	.	Offset 800	.	Offset 1000
.		.		.	
.		.		.	
01F8		0EF8		17F8	
01FC		0EFC		17FC	

The memory map of each module type is described hereafter:

A/D (MODULE C)



A/D channels use individual A/D converters with a high (200 kHz) sampling rate per channel. The input range and gain is field programmable for each channel. Each of these differential channels includes a second order anti-aliasing filter and a post filter that has a digitally programmable break point that enables user to field adjust the filtering for each channel. All A/D channels are self-calibrating because each channel, on a rotating basis, is automatically calibrated to eliminate offset and gain errors. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution (does not apply to Current Measurement Module C3 which is fixed unipolar, 0-25mA FS). Open inputs cannot be sensed because scaling input resistor networks are used. All inputs are double buffered for immediate availability. The "Latch" feature permits the user to read all A/D channels at the same time.

The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 0.2% FS. Any failure triggers an Interrupt (if enabled) with the results available in BIT status register. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

In addition, all channels are monitored for open input (except for Current Measurement Module C3 applications).

The (D3) test starts an initiated BIT test that disconnects all A/D's from the I/O and then connects them across an internal stimulus. Each channel will be checked to a test accuracy of 0.2% FS and monitored for open inputs. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from "1" to "0". The test can be stopped at any time and requires no user programming and can be enabled or disabled via the bus.

A (D0) test is used to check the card and PCI interface. Write "1" to D0 of *Test enable* register to disconnect all A/D channels from the I/O and connects them across an internal D/A. Test parameters are controlled by the user and are entered in the *D0 Test Voltage* and *DO Test Range* registers. The outputs from the A/D channels are monitored by an internal D/A for proper conversion. External reference voltage is not required

A/D Open Circuit monitoring is disabled during D3 testing.

Note: A/D differential inputs must not "float" (i.e. common mode voltage as referenced to PCI system ground must not exceed maximum specifications for the module).

A/D MODULE MEMORY MAP

000	Data 1	R	028	Range & Polarity[1] 1	R/W	050	Filter Break Freq. 1	R/W	200	CH1 FIFO Buffer Data	R
004	Data 2	R	02C	Range & Polarity 2	R/W	054	Filter Break Freq. 2	R/W	204	CH2 FIFO Buffer Data	R
008	Data 3	R	030	Range & Polarity 3	R/W	058	Filter Break Freq. 3	R/W	208	CH3 FIFO Buffer Data	R
00C	Data 4	R	034	Range & Polarity 4	R/W	05C	Filter Break Freq. 4	R/W	20C	CH4 FIFO Buffer Data	R
010	Data 5	R	038	Range & Polarity 5	R/W	060	Filter Break Freq. 5	R/W	210	CH5 FIFO Buffer Data	R
014	Data 6	R	03C	Range & Polarity 6	R/W	064	Filter Break Freq. 6	R/W	214	CH6 FIFO Buffer Data	R
018	Data 7	R	040	Range & Polarity 7	R/W	068	Filter Break Freq. 7	R/W	218	CH7 FIFO Buffer Data	R
01C	Data 8	R	044	Range & Polarity 8	R/W	06C	Filter Break Freq. 8	R/W	21C	CH8 FIFO Buffer Data	R
020	Data 9	R	048	Range & Polarity 9	R/W	070	Filter Break Freq. 9	R/W	220	CH9 FIFO Buffer Data	R
024	Data 10	R	04C	Range & Polarity 10	R/W	074	Filter Break Freq. 10	R/W	224	CH10 FIFO Buffer Data	R
240	CH1 FIFO words	R	280	CH1 Hi-Threshold	R/W	2C0	CH1 Lo-Threshold	R/W	300	CH1 Delay	R/W
244	CH2 FIFO words	R	284	CH2 Hi-Threshold	R/W	2C4	CH2 Lo-Threshold	R/W	304	CH2 Delay	R/W
248	CH3 FIFO words	R	288	CH3 Hi-Threshold	R/W	2C8	CH3 Lo-Threshold	R/W	308	CH3 Delay	R/W
24C	CH4 FIFO words	R	28C	CH4 Hi-Threshold	R/W	2CC	CH4 Lo-Threshold	R/W	30C	CH4 Delay	R/W
250	CH5 FIFO words	R	290	CH5 Hi-Threshold	R/W	2D0	CH5 Lo-Threshold	R/W	310	CH5 Delay	R/W
254	CH6 FIFO words	R	294	CH6 Hi-Threshold	R/W	2D4	CH6 Lo-Threshold	R/W	314	CH6 Delay	R/W
258	CH7 FIFO words	R	298	CH7 Hi-Threshold	R/W	2D8	CH7 Lo-Threshold	R/W	318	CH7 Delay	R/W
25C	CH8 FIFO words	R	29C	CH8 Hi-Threshold	R/W	2DC	CH8 Lo-Threshold	R/W	31C	CH8 Delay	R/W
260	CH9 FIFO words	R	2A0	CH9 Hi-Threshold	R/W	2E0	CH9 Lo-Threshold	R/W	320	CH9 Delay	R/W
264	CH10 FIFO words	R	2A4	CH10 Hi-Threshold	R/W	2E4	CH10 Lo-Threshold	R/W	324	CH10 Delay	R/W
340	CH1 FIFO size	R/W	380	CH1 Sample Rate	R/W	3C0	CH1 Clear FIFO	R/W	400	CH1 Buffer Control	R/W
344	CH2 FIFO size	R/W	384	CH2 Sample Rate	R/W	3C4	CH2 Clear FIFO	R/W	404	CH2 Buffer Control	R/W
348	CH3 FIFO size	R/W	388	CH3 Sample Rate	R/W	3C8	CH3 Clear FIFO	R/W	408	CH3 Buffer Control	R/W
34C	CH4 FIFO size	R/W	38C	CH4 Sample Rate	R/W	3CC	CH4 Clear FIFO	R/W	40C	CH4 Buffer Control	R/W
350	CH5 FIFO size	R/W	390	CH5 Sample Rate	R/W	3D0	CH5 Clear FIFO	R/W	410	CH5 Buffer Control	R/W
354	CH6 FIFO size	R/W	394	CH6 Sample Rate	R/W	3D4	CH6 Clear FIFO	R/W	414	CH6 Buffer Control	R/W
358	CH7 FIFO size	R/W	398	CH7 Sample Rate	R/W	3D8	CH7 Clear FIFO	R/W	418	CH7 Buffer Control	R/W
35C	CH8 FIFO size	R/W	39C	CH8 Sample Rate	R/W	3DC	CH8 Clear FIFO	R/W	41C	CH8 Buffer Control	R/W
360	CH9 FIFO size	R/W	3A0	CH9 Sample Rate	R/W	3E0	CH9 Clear FIFO	R/W	420	CH9 Buffer Control	R/W
364	CH10 FIFO size	R/W	3A4	CH10 Sample Rate	R/W	3E4	CH10 Clear FIFO	R/W	424	CH10 Buffer Control	R/W
440	CH1 Trig Control	R/W	480	CH1 FIFO Status	R/W	4C0	CH1 Interrupt Status	R/W	500	Software Trigger	R/W
444	CH2 Trig Control	R/W	484	CH2 FIFO Status	R/W	4C4	CH2 Interrupt Status	R/W	504	Clk Rate Adder Input Hi	R/W
448	CH3 Trig Control	R/W	488	CH3 FIFO Status	R/W	4C8	CH3 Interrupt Status	R/W	508	Clk Rate Adder Input Lo	R/W
44C	CH4 Trig Control	R/W	48C	CH4 FIFO Status	R/W	4CC	CH4 Interrupt Status	R/W	510	Rate Mode Control	R/W
450	CH5 Trig Control	R/W	490	CH5 FIFO Status	R/W	4D0	CH5 Interrupt Status	R/W			
454	CH6 Trig Control	R/W	494	CH6 FIFO Status	R/W	4D4	CH6 Interrupt Status	R/W	6F8	A/D Test Enable	R/W
458	CH7 Trig Control	R/W	498	CH7 FIFO Status	R/W	4D8	CH7 Interrupt Status	R/W	700	BIT Status Ch.1-10	R
45C	CH8 Trig Control	R/W	49C	CH8 FIFO Status	R/W	4DC	CH8 Interrupt Status	R/W	704	Open Status[2] Ch.1-10	R
460	CH9 Trig Control	R/W	4A0	CH9 FIFO Status	R/W	4E0	CH9 Interrupt Status	R/W	708	BIT Stat Interrupt Enable Ch.1-10	R/W
464	CH10 Trig Control	R/W	4A4	CH10 FIFO Status	R/W	4E4	CH10 Interrupt Status	R/W	70C	Open Stat INTR Enable Ch.1-10	R/W
						1E0	A/D Latch	R/W	768	Module Design Version	R
						1E4	D0 Test Range	R/W	76C	Module Design Revision	R
						1E8	D0 Test Voltage	R/W	770	Module DSP	R
									774	Module FPGA	R
									778	Module ID	R
									7C0	BIT Interrupt Vector	R/W
									7C4	Open Status Interrupt Vector	R/W

Note: 1. Range & Polarity Register is simply called Range Register in software driver/library.
Range & Polarity does not apply to Current Measurement Module C3
2. Open Status does NOT apply to High Voltage (20V to 80V), or Current Measurement modules.

Data Read

Two's complement format for bipolar mode; 7FFFh=+FS, 8,000h=-FS. For unipolar mode, range is from 0h to FFFFh = FS.

A/D Range & Polarity

Format input for range and polarity. Range is dependent upon Module. Encode range using data bits D0 through D3. Program polarity using data bit D4. Enter per table. Does not apply to Current Measurement Module (C3 is fixed unipolar, 0-25mA FS).

REGISTER	D15	D1	D1	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RANGE & POLARITY	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**

MODULE	C4	C2	C1					
Uni-polar RANGE	0 – 50.0 V	0 – 40.0 V	N/A	**0**	**1**	**0**	**1**	**0**
	0 – 25.0 V	0 – 20.0 V	N/A	**0**	**1**	**0**	**0**	**1**
	0 – 12.5 V	0 – 10.0 V	0 – 10.0 V	**0**	**0**	**0**	**0**	**0**
	0 – 6.25 V	0 – 5.00 V	0 – 5.00 V	**0**	**0**	**0**	**0**	**1**
	N/A	N/A	0 – 2.50 V	**0**	**0**	**0**	**1**	**0**
	N/A	N/A	0 – 1.25 V	**0**	**0**	**0**	**1**	**1**
	N/A	N/A	N/A	**0**	**0**	**1**	**0**	**0**
Bipolar RANGE	±50.0 V	±40.0 V	N/A	**1**	**1**	**0**	**1**	**0**
	±25.0 V	±20.0 V	N/A	**1**	**1**	**0**	**0**	**1**
	±12.5 V	±10.0 V	±10.0 V	**1**	**0**	**0**	**0**	**0**
	±6.25 V	±5.00 V	±5.00 V	**1**	**0**	**0**	**0**	**1**
	N/A	N/A	±2.50 V	**1**	**0**	**0**	**1**	**0**
	N/A	N/A	±1.25 V	**1**	**0**	**0**	**1**	**1**

A/D Filter Break Frequency

The break frequency is the 3 db point of a single pole low pass filter. Enter desired frequency for each channel between 10 Hz to 10 kHz as a 16 bit binary number. Zero disables filter.

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN VERSION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP
Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA
Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID
Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4331h

Read register to determine Module ID in ASCII. For example, find ASCII "C" in upper byte and ASCII "1" in lower byte, for Module "C1," together 4331h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "C"								ASCII "1"								

BIT Status
Check the corresponding bit for a channel's BIT Status. A "0" =Normal; "1" = Non-compliant A/D conversion (outside 0.2% FS accuracy spec). Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status
Check for an open or disconnect to the A/D input. Status of each channel is indicated at its corresponding bit. A "0" =Normal and "1" = Open. An open or disconnect to the input of an A/D channel is detected within 10 seconds and will latch the corresponding bit in the *Open Status* register. Reading any status bit will unlatch the entire register. Open Status is part of background testing and the status register may be checked or polled at any given time. NOTE: Does not apply to Current Measurement Module C3.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status	X	X	X	X	X	X	Ch. 10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable
Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status Interrupt Enable
Set the bit to enable interrupts for the corresponding channel monitored for Open Status. Open Status does NOT apply to high voltage (20V to 80V) or current measurement modules.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Latch All A/Ds

Latch all A/D channels by writing “1” to D1 of Latch register. Write “0” to unlatch all channels.

A/D D0 Test Range

Specify voltage range for A/D module under test. D0 test is performed only on A/D modules. Enter per table.
NOTE: for Current Measurement Module C3, enter up to 2.5V for 25mA FS, unipolar selection only.

REGISTER	D15	D1	D1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A/D D0 TEST RANGE	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**

MODULE	C4	C2	C1					
RANGE	50.0 V	40.0 V	40.0 V	*	**1**	**0**	**1**	**0**
	25.0 V	20.0 V	20.0 V	*	**1**	**0**	**0**	**1**
	12.5 V	10.0 V	10.0 V	*	**0**	**0**	**0**	**0**
	6.25 V	5.00 V	5.00 V	*	**0**	**0**	**0**	**1**
			2.50 V	*	**0**	**0**	**1**	**0**
			1.25 V	*	**0**	**0**	**1**	**1**

∗ For bipolar/uni-polar selection, program D4 as “0” for unipolar and “1” for bipolar.

A/D D0 Test Voltage

Specify voltage to be applied by D0 test to A/D module under test. D0 test is performed only on A/D modules. If using bi-polar mode, write 16 bit 2’s complement word (7FFFh=+FS, 8000h=-FS). If using uni-polar mode, write 16 bit binary word (range: 0 to FFFFh=FS).

Example 1: if using uni-polar mode with 10v range, enter 8000h for 5v test voltage.
Example 2: if using bi-polar mode with 10v range, enter 4000h for 5v test voltage. Enter C000h for –5v.

A/D FIFO Buffer Operational Description

A/D Data:
The available data in the FIFO buffer can be retrieved in the following PCI memory addresses one "WORD"(16bits) at a time. The data is presented in two's complement format depending on the range and polarity setting of the individual channel. For bipolar mode; 7FFFh=+FS, 8,000h=-FS. For unipolar mode, range is from 0h to FFFFh = FS.

Addr	r / w	Description	A/D Data(16Bit hex)
200	r	data ch1	Data Range: (0x0000-0xFFFF)
204	r	data ch2	
208	r	data ch3	
20C	r	data ch4	
210	r	data ch5	
214	r	data ch6	
218	r	data ch7	
21C	r	data ch8	
220	r	data ch9	
224	r	data ch10	

Words in FIFO:
This is a counter that revolves the number of data in WORD(2 byte) stored in the FIFO buffer. Every time when a read operation is made to the A/D Data memory address, its corresponding "Words in FIFO" counter will be decremented by one. The maximum number of words can be stored in the FIFO is 26,213(0x6665).

Addr	r / w	Description	Words in FIFO(16Bit hex)
240	r	Words in ch1	Data Range: (0x0000-0x6665)
244	r	Words in ch2	
248	r	Words in ch3	
24C	r	Words in ch4	
250	r	Words in ch5	
254	r	Words in ch6	
258	r	Words in ch7	
25C	r	Words in ch8	
260	r	Words in ch9	
264	r	Words in ch10	

Hi-Threshold:
The hi-threshold level is used to set or reset the high limit bit(B2) of the individual channel status register in PCI memory location. When the "Words in FIFO" counter is greater than the value stored in the hi-threshold register, the high limit bit (B2) of the channel status register will be set. When the "Words in FIFO" counter is less than or equal to the value stored in the hi-threshold, the high limit bit (B2) of the channel status register will be reset.
Set = "logical 1"
Reset = "logical 0"

Addr	r / w	Description	Hi-Threshold(16Bit hex)
280	rw	Hi-Threshold in ch1	Data Range: (0x0000-0x6665)
284	rw	Hi-Threshold in ch2	
288	rw	Hi-Threshold in ch3	
28C	rw	Hi-Threshold in ch4	
290	rw	Hi-Threshold in ch5	
294	rw	Hi-Threshold in ch6	
298	rw	Hi-Threshold in ch7	
29C	rw	Hi-Threshold in ch8	
2A0	rw	Hi-Threshold in ch9	
2A4	rw	Hi-Threshold in ch10	

Low-Threshold:
The low-threshold level is used to set or reset the low limit bit (B1) of the individual channel status register in PCI memory location. When the "Words in FIFO" counter is greater than or equal to the value stored in the low-threshold, the low limit bit (B1) of the channel status register will be reset. When the "Words in FIFO" counter is less than the value stored in the low-threshold, the low limit bit (B1) of the channel status register will be set.
Set = "logical 1"
Reset = "logical 0"

Addr	r / w	Description	Low-Threshold(16Bit hex)
2C0	rw	Low-Threshold in ch1	Data Range: (0x0000-0x6665)
2C4	rw	Low-Threshold in ch2	
2C8	rw	Low-Threshold in ch3	
2CC	rw	Low-Threshold in ch4	
2D0	rw	Low-Threshold in ch5	
2D4	rw	Low-Threshold in ch6	
2D8	rw	Low-Threshold in ch7	
2DC	rw	Low-Threshold in ch8	
2E0	rw	Low-Threshold in ch9	
2E4	rw	Low-Threshold in ch10	

Delay:
Set the number of delay samples before the actual FIFO data collection begins. The data collected during the delay period will be discarded.

Addr	r / w	Description	Delay(16Bit hex)
300	rw	Delay in ch1	Data Range: (0x0000-0xFFFF)
304	rw	Delay in ch2	
308	rw	Delay in ch3	
30C	rw	Delay in ch4	
310	rw	Delay in ch5	
314	rw	Delay in ch6	
318	rw	Delay in ch7	
31C	rw	Delay in ch8	
320	rw	Delay in ch9	
324	rw	Delay in ch10	

Size:
Set the size of the FIFO buffer. The largest size that a FIFO buffer can be is 26,213(0x6665)

Addr	r / w	Description	Size(16Bit hex)
340	rw	Size in ch1	Data Range: (0x0000-0x6665)
344	rw	Size in ch2	
348	rw	Size in ch3	
34C	rw	Size in ch4	
350	rw	Size in ch5	
354	rw	Size in ch6	
358	rw	Size in ch7	
35C	rw	Size in ch8	
360	rw	Size in ch9	
364	rw	Size in ch10	

Sample Rate:
The sample rate sets the sampling rate for the FIFO buffer. The rate is based on the product of 5e-6 second x Sample Rate. For example, if the address(0x1C0) is set to 2, the FIFO buffer will be sampling at 5e-6 * 2 = 10e-6 seconds.

Addr	r / w	Description	Sample Rate(16Bit hex)
380	rw	Rate in ch1	Data Range: (0x0000-0xFFFF)
384	rw	Rate in ch2	
388	rw	Rate in ch3	
38C	rw	Rate in ch4	
390	rw	Rate in ch5	
394	rw	Rate in ch6	
398	rw	Rate in ch7	
39C	rw	Rate in ch8	
3A0	rw	Rate in ch9	
3A4	rw	Rate in ch10	

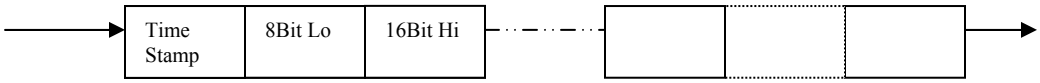
Clear FIFO:
Whenever the Clear memory is set or reset for the individual channel, it initializes the “Words in FIFO” to zero. A read to the “A/D Data” register gives aged data.

Addr	r / w	Description	Clear FIFO(16Bit hex)
3C0	rw	Clear in ch1	Data Range: (0x0000-0xFFFF)
3C4	rw	Clear in ch2	
3C8	rw	Clear in ch3	
3CC	rw	Clear in ch4	
3D0	rw	Clear in ch5	
3D4	rw	Clear in ch6	
3D8	rw	Clear in ch7	
3DC	rw	Clear in ch8	
3E0	rw	Clear in ch9	
3E4	rw	Clear in ch10	

Buffer Control:
Different types of data format can be stored in the FIFO buffer and their formats are defined by the Buffer Control Register. The following bit mask defines the type/format of data that will be put into the FIFO buffer.

B0 = Data(16 Bit Hi). 16 bit resolution data for unipolar and bipolar.
B1 = Data(8 Bit Lo). Combine with B0 to form a 24 bit resolution for unipolar and bipolar data.
B2 = Filtered Data(16 Bit Hi). Filtered 16 bit resolution data for unipolar and bipolar.
B3 = Filtered Data(8 Bit Lo). Combine with B2 to form a 24 bit resolution for both unipolar and bipolar data.
B4 = Time Stamp. An integer counter that counts from 0 to 65535 and wraps around when it overflows.
B5 = Reserved
B6 = Reserved
B7 = Reserved

Note: Each data format (B0 – B4) requires one word of storage space from the FIFO buffer. For example, if B0, B1 and B4 are set(0x13) and the Size register is set to 1, a FIFO write will put 3 words of data to the FIFO memory spaces. Since the maximum physical size of FIFO is 26,213 for each channel, the value in the Size and Buffer Control register could cause an overflow to the FIFO buffer. When an overflow condition occurred, any un-stored data will be lost.



FIFO Buffer For Each Write

Addr	r / w	Description	Buffer Ctrl.(16Bit hex)
400	rw	Buf. Ctrl. in ch1	Data Range: b0-b4
404	rw	Buf. Ctrl. in ch2	
408	rw	Buf. Ctrl. in ch3	
40C	rw	Buf. Ctrl. in ch4	
410	rw	Buf. Ctrl. in ch5	
414	rw	Buf. Ctrl. in ch6	
418	rw	Buf. Ctrl. in ch7	
41C	rw	Buf. Ctrl. in ch8	
420	rw	Buf. Ctrl. in ch9	
424	rw	Buf. Ctrl. in ch10	

Trigger Control:
The FIFO can be started/triggered by different sources.
B0-B1 = Source Select(choose one only)
0x0 = Ext. Trigger 2
0x1 = Ext. Trigger 1
0x2 = Software Trigger
B3 = Reserved
B4-B7 = Trigger Type(Choose one only)
0x10 = Negative Slope
0x20 = Trigger Pulse Enable
0x40 = Trigger Pulse/Trigger Enable Select
0x80 = Trigger Clear

Addr	r / w	Description	Trigger Ctrl.(16Bit hex)
440	rw	Trigger Ctrl. in ch1	Data Range: b0-b7
444	rw	Trigger Ctrl. in ch2	
448	rw	Trigger Ctrl. in ch3	
44C	rw	Trigger Ctrl. in ch4	
450	rw	Trigger Ctrl. in ch5	
454	rw	Trigger Ctrl. in ch6	
458	rw	Trigger Ctrl. in ch7	
45C	rw	Trigger Ctrl. in ch8	
460	rw	Trigger Ctrl. in ch9	
464	rw	Trigger Ctrl. in ch10	

FIFO Status:
The FIFO status register indicates the current condition of the FIFO buffer. B0-B4 is used to show the different condition of the buffer.
B0 = Empty. When “Words In FIFO” register is zero, B0 = 1; otherwise =B0 =0.
B1 = Low Limit. When “Words In FIFO” register” < “Low-Threshold”, B1= 1; otherwise B1 =0.
B2 = High Limit. When “Words In FIFO” register” > “Hi-Threshold”, B2=1; otherwise B2 =0.
B3 = FIFO Full. When “Words In FIFO” register” = 26213, B3=1; otherwise B3 =0.
B4 = Sample Done. When “Words In FIFO” register = “Size”, B4=1; otherwise B4 =0.

Addr	r / w	Description	FIFO Status(16Bit hex)
480	r	Status in ch1	Data Range: b0-b4
484	r	Status in ch2	
488	r	Status in ch3	
48C	r	Status in ch4	
490	r	Status in ch5	
494	r	Status in ch6	
498	r	Status in ch7	
49C	r	Status in ch8	
4A0	r	Status in ch9	
4A4	r	Status in ch10	

Interrupt:
To be determined.

Addr	r / w	Description	FIFO Status(16Bit hex)
4C0	rw	Status in ch1	Data Range: 0x0-0xFFFF
4C4	rw	Status in ch2	
4C8	rw	Status in ch3	
4CC	rw	Status in ch4	
4D0	rw	Status in ch5	
4D4	rw	Status in ch6	
4D8	rw	Status in ch7	
4DC	rw	Status in ch8	
4E0	rw	Status in ch9	
4E4	rw	Status in ch10	

Software Trigger:
Software trigger is used to kick start the FIFO buffer and collection of data. In order to use this operation, the "Trigger Ctrl" register must be set up properly. Setting or resetting the "Software Trigger" will start FIFO data collection for ALL channels.

Addr	R / w	Description	Software Trigger(16Bit hex)
500	rw	Software Trigger	Data Range: 0x0-0xFFFF

Clock Rate Adder Input Hi:
To be determined.

Addr	R / w	Description	Software Trigger(16Bit hex)
504	rw	Clk Rate Adder Input Hi	Data Range: 0x0-0xFFFF

Clock Rate Adder Input Low:
To be determined.

Addr	R / w	Description	Software Trigger(16Bit hex)
508	rw	Clk Rate Adder Input Low	Data Range: 0x0-0xFFFF

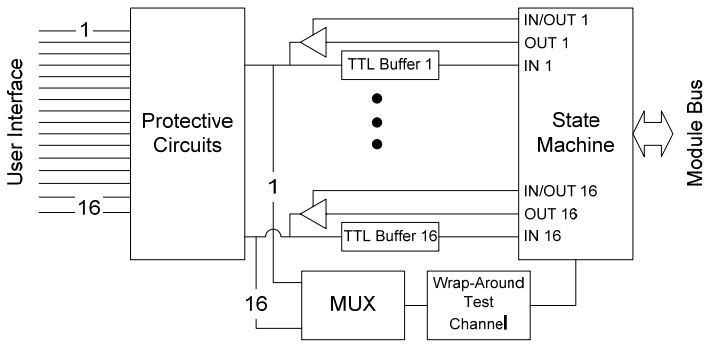
Rate Mode Control:
Use to set the sample rate of the A/D converter.
B0-B1: 0x0 = 195.3 kHz
0x1 = 97.7 kHz
0x2 = 48.8 kHz
0x3 = 44.1 kHz

Addr	R / w	Description	Software Trigger(16Bit hex)
510	rw	Rate Mode Control	Data Range: 0x0-0xFFFF

I/O DIGITAL TTL, (MODULE D7)

Digital (TTL) I/O channels (in banks of 16) are programmable for either Input or Output and include extensive diagnostics. Interrupt can be selected, for each channel, to indicate transition on rising edge, transition on falling edge, or both. De-bounce circuits for each channel offer a selectable time delay to eliminate false signals resulting from contact bounce commonly experienced with mechanical relays and switches. Each TTL channel has an internal 110KΩ pull-down resistor. All inputs are continually scanned and the data is double buffered for immediate availability.

TTL Module Block Diagram



The (D2) test initiates **automatic** background BIT testing which tests and validates channel processing (data read or write logic), tests for circuit over-current conditions and provides status for threshold signal transitioning. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus.

I/O DIGITAL (TTL) D1 MODULE MEMORY MAP

000	Write Output,	Ch.1-16 R/W	0E0	Debounce time	Ch.11 R/W	1A0	Status Fault	Ch.01-16	R
004	Read I/O,	Ch.1-16 R/W	0F4	Debounce time	Ch.12 R/W	1A8	Status Over-Current	Ch.01-16	R
018	Debounce time	Ch.1 R/W	108	Debounce time	Ch.13 R/W	1B8	Status Lo-Hi Transition	Ch.01-16	R
02C	Debounce time	Ch.2 R/W	11C	Debounce time	Ch.14 R/W	1BC	Status Hi-Lo Transition	Ch.01-16	R
040	Debounce time	Ch.3 R/W	130	Debounce time	Ch.15 R/W	000	Interrupt Fault Enable	Ch.01-16	R/W
054	Debounce time	Ch.4 R/W	144	Debounce time	Ch.16 R/W	1D8	Interrupt Over-Current Enable	Ch.01-16	R/W
068	Debounce time	Ch.5 R/W	148	Input/Output Format	Ch.01-8 R/W	1E8	Interrupt Lo-Hi Transition Enable	Ch.01-16	R/W
07C	Debounce time	Ch.6 R/W	14C	Input/Output Format	Ch.09-16 R/W	1EC	Interrupt Hi-Lo Transition Enable	Ch.01-16	R/W
090	Debounce time	Ch.7 R/W	178	Reset Over-Current	Ch.1-16 R/W				
0A4	Debounce time	Ch.8 R/W				768	Module Design Version[1]		R
0B8	Debounce time	Ch.9 R/W				76C	Module Design Revision[1]		R
0CC	Debounce time	Ch.10 R/W				770	Module DSP[1]		R
						774	Module FPGA[1]		R
						778	Module ID		R

Note: 1. Pending

Write Output

When a channel is configured for Output, write logic level High (“1”) or Low (“0”) to associated channel bit, in 16 bit binary word. Each bit corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Read I/O

Independent of channel configuration (Input or Output), read logic state High (“1”) or Low (“0”) as defined by channel threshold values. Each bit of 16-bit binary word corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

De-bounce time

Enter required de-bounce time into appropriate channel registers. Enter time in 1.28μs increments, up to 326.40 μsec. LSB= 1.28 μs. Value is 8 bits (MSBs=don't care). Once a signal level is a logic voltage level period longer than the De-bounce time (Logic High > 2.0 v, and Logic Low < 0.6 v), a logic transition is validated. Signal pulse widths less than De-bounce time are filtered or ignored. Once valid, the interrupt transition register channel flag is set and the output logic changes state. Enter a value of 0 to disable De-bounce filtering. De-bounce defaults to 00h upon reset.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
									163.84	81.92	40.96	20.48	10.24	5.12	2.56	1.28	value in mSec (LSB=1.28μS)
DE-BOUNCE TIME	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input/Output Format

Configure channels in groups of 8. Write integer 0 for input, 3 for output: Default is configured for Input.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INPUT/OUTPUT CH 01-08	Ch.08		Ch.07		Ch.06		Ch.05		Ch.04		Ch.03		Ch.02		Ch.01		Channel
INPUT/OUTPUT CH 09-16	Ch.16		Ch.15		Ch.14		Ch.13		Ch.12		Ch.11		Ch.10		Ch.09		Channel
INPUT/OUTPUT	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT

Integer	D_H	D_L	
0	**0**	**0**	Input
3	**1**	**1**	Output

Reset Over-Current

Write integer "1" to reset all sixteen channels (per module). Used to reset disabled channel(s) following an over-current condition. When reset process is complete, processor will write a "0" back to the *Reset Over-Current* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESET OVER-CURRENT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	D=DATA BIT

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN VERSION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4431h

Read register to determine Module ID in ASCII. For example, find ASCII "D" in upper byte and ASCII "1" in lower byte for Module "D1," together 4431h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "D"								ASCII "1"								

Automatic background BIT testing

BIT is always enabled and continually checks that each channel is functional. This capability is accomplished by an additional test comparator that is incorporated into each 16 channel module. The test comparator is sequentially connected across each channel and is compared against the operational channel. Depending upon configuration, the Input data read or Output logic write of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. Low to High and High to Low logic transitions are indicated. Additional testing of output logic indicates Over-current condition when output logic is invalid for a period greater than 80µs.

Status indications

Fault – processing (data read or write logic) is inconsistent with redundant test circuit.
Status is indicated within 15 seconds. A fault is latched until read. (Testing takes approx. 1 second per channel)

Lo-Hi Transition – If a Lo to High transition is sensed, status is indicated (bit is set) within 40µs.
Hi-Low Transition – If a High to Low transition is sensed, status is indicated (bit is set) within 40µs.

Over-current – If over-current or overload condition is sensed, status is indicated (bit is set) within 80µs.
Output is however, immediately disabled at time of over-current condition.

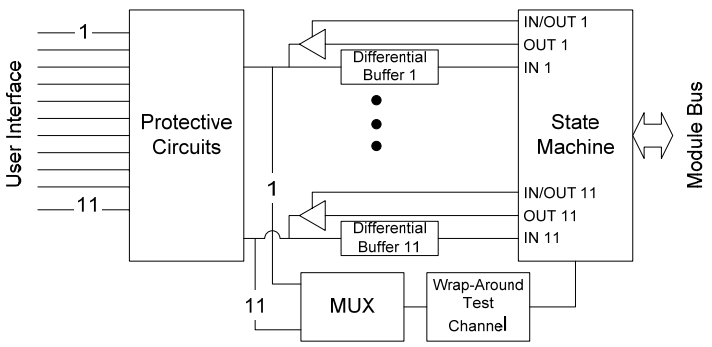
When status is "indicated," or bit is "set," bit value is logic "1." Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

I/O DIGITAL DIFFERENTIAL MULTI-MODE TRANSCEIVERS (MODULE D8)

Differential RS422/RS485 I/O channels (in banks of 11) are programmable for either Input or Output and include extensive diagnostics. Each Differential input channel has a selectable internal resistor (120Ω or >12kΩ) across its inputs. Interrupt can be selected, for each channel, to indicate transition on rising edge, transition on falling edge, or both. De-bounce circuits for each channel offer a selectable time delay to eliminate false signals resulting from contact bounce commonly experienced with mechanical relays and switches. All inputs are continually scanned and the data is double buffered for immediate availability.

Differential Module Block Diagram



The (D2) test initiates **automatic** background BIT testing which tests and validates channel processing (data read or write logic), tests for circuit over-current conditions and fault status. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus.

I/O DIGITAL (TTL) D2 MODULE MEMORY MAP

000	Write Output,	Ch.1-11 R/W	0B8	Debounce time	Ch.9 R/W	1A0	Status Fault	Ch.01-11	R
004	Read I/O,	Ch.1-11 R/W	0CC	Debounce time	Ch.10 R/W	1A8	Status Over-Current	Ch.01-11	R
018	Debounce time	Ch.1 R/W	0E0	Debounce time	Ch.11 R/W	1B8	Status Lo-Hi Transition	Ch.01-11	R
02C	Debounce time	Ch.2 R/W	144	Input Termination	Ch 01-11 R/W	1BC	Status Hi-Lo Transition	Ch.01-11	R
040	Debounce time	Ch.3 R/W	148	Input/Output Format	Ch.1-8 R/W	000	Interrupt Fault Enable	Ch.01-11	R/W
054	Debounce time	Ch.4 R/W	14C	Input/Output Format	Ch.9-11 R/W	1D8	Interrupt Over-Current Enable	Ch.01-11	R/W
068	Debounce time	Ch.5 R/W				1E8	Interrupt Lo-Hi Transition Enable	Ch.01-11	R/W
07C	Debounce time	Ch.6 R/W				1EC	Interrupt Hi-Lo Transition Enable	Ch.01-11	R/W
090	Debounce time	Ch.7 R/W							
0A4	Debounce time	Ch.8 R/W				768	Module Design Version[1]		R
						76C	Module Design Revision[1]		R
						770	Module DSP[1]		R
						774	Module FPGA[1]		R
						778	Module ID		R

Note: 1. Pending

Write Output

When a channel is configured for Output, write logic level High (“1”) or Low (“0”) to associated channel bit, in 16 bit binary word. Each bit corresponds to one of 11 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
						11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Read I/O

Independent of channel configuration (Input or Output), read logic state High (“1”) or Low (“0”). Each bit of 16-bit binary word corresponds to one of 11 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
						11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

De-bounce time

Enter required de-bounce time into appropriate channel registers. Enter time in 1.28μs increments, up to 326.40 μsec. LSB= 1.28 μs. Value is 8 bits (MSBs=don't care). Once a signal level is a logic voltage level period longer than the De-bounce time (Logic High > 2.0 v, and Logic Low < 0.6 v), a logic transition is validated. Signal pulse widths less than De-bounce time are filtered or ignored. Once valid, the interrupt transition register channel flag is set and the output logic changes state. Enter a value of 0 to disable De-bounce filtering. De-bounce defaults to 00h upon reset.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
									163.84	81.92	40.96	20.48	10.24	5.12	2.56	1.28	value in mSec (LSB=1.28μS)
DE-BOUNCE TIME	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input Termination Control

Each differential input pair can be programmed to have an input termination of 120 Ω or >12k Ω. Write logic'1' to select 120 Ω for each individual channel. Default is >12k Ω.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
						11	10	9	8	7	6	5	4	3	2	1	Channel
INPUT TERMINATION	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input/Output Format

Write integer 0 for input, 3 for output: Default is configured for Input.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INPUT/OUTPUT CH 01-08	Ch.08		Ch.07		Ch.06		Ch.05		Ch.04		Ch.03		Ch.02		Ch.01		Channel
INPUT/OUTPUT CH 09-11											Ch.11		Ch.10		Ch.09		Channel
INPUT/OUTPUT	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT

Integer	D_H	D_L	
0	**0**	**0**	Input
3	**1**	**1**	Output

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4332h

Read register to determine Module ID in ASCII. For example, find ASCII “D” in upper byte and ASCII “2” in lower byte for Module “D2,” together 4432h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “D”								ASCII “2”								

Automatic background BIT testing

BIT is always enabled and continually checks that each channel is functional. This capability is accomplished by an additional test comparator that is incorporated into each 11 channel module. The test comparator is sequentially connected across each channel and is compared against the operational channel. Depending upon configuration, the Input data read or Output logic write of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. Low to High and High to Low logic transitions are indicated. Additional testing of output logic indicates Over-current condition when output logic is invalid for a period greater than 80µs.

Status indications

Fault – processing (data read or write logic) is inconsistent with redundant test circuit.
Status is indicated within 15 seconds. A fault is latched until read. (Testing takes approx. 1 second per channel)

Lo-Hi Transition – If a Lo to High transition is sensed, status is indicated within 40µs.
Hi-Low Transition – If a High to Low transition is sensed, status is indicated within 40µs.

Over-current – If over-current or overload condition is sensed, status is indicated (bit is set) within 80µs.
Output is however, immediately disabled at time of over-current condition. Over-current is re-checked every 6ms. If applicable output is re-enabled and channel is reset.

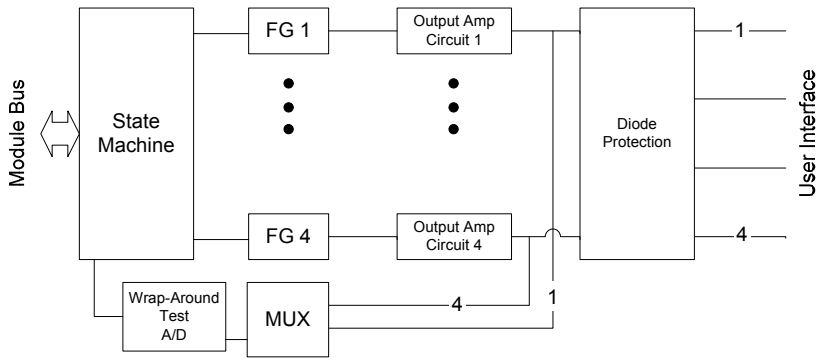
A ”0” indicates Passing and “1” Failing status. Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

SIGNAL GENERATOR (MODULE E5)

Signal Generator modules generate one of a selection of waveforms, sine, triangular, or square wave, per channel, programmable in frequency and amplitude. Use of an individual A/D self test channel, on a rotating basis, verifies that the channel is operating properly in frequency, amplitude, and DC offset. See wrap-around test registers for BIT data

Signal Module Block Diagram



Operating at all times is a background Built-In-Test (BIT), where each channel is checked to a test accuracy of 2% FS. Any failure triggers an Interrupt (if enabled) with the results available in status registers. BIT is intended for use with steady state signals; any change in channel configuration (amplitude, frequency, etc) requires up to 12 seconds before wrap data reflects that change. Multiple changes in channel configuration in less than 12 seconds may trigger false BIT failures. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card.

SIGNAL GENERATOR (E) MODULE MEMORY MAP

000	Ch.1 Frequency High	R/W	040	Ch.3 DC Offset	R/W	0A0	Ch.3 Wrap-around Frequency High	R
004	Ch.1 Frequency Low	R/W	044	Ch.3 Mode	R/W	0A4	Ch.3 Wrap-around Frequency Low	R
008	Not used		048	Ch.4 Freq Hi	R/W	0A8	Ch.3 Wrap-around Amplitude	R
00C	Ch.1 Amplitude	R/W	04C	Ch.4 Freq Lo	R/W	0AC	Ch.3 Wrap-around DC Offset	R
010	Ch.1 DC Offset	R/W	050	Ch.4 Phase	R/W	0B0	Ch.4 Wrap-around Frequency High	R
014	Ch.1 Mode	R/W	054	Ch.4 Amplitude	R/W	0B4	Ch.4 Wrap-around Frequency Low	R
018	Ch.2 Freq Hi	R/W	058	Ch.4 DC Offset	R/W	0B8	Ch.4 Wrap-around Amplitude	R
01C	Ch.2 Freq Lo	R/W	05C	Ch.4 Mode	R/W	0BC	Ch.4 Wrap-around DC Offset	R
020	Ch.2 Phase	R/W	080	Ch.1 Wrap-around Frequency High	R			
024	Ch.2 Amplitude	R/W	084	Ch.1 Wrap-around Frequency Low	R	1A0	BIT Status Ch.1-4	R
028	Ch.2 DC Offset	R/W	088	Ch.1 Wrap-around Amplitude	R	1C0	BIT Stat Interrupt Enable Ch.1-4	R/W
02C	Ch.2 Mode	R/W	08C	Ch.1 Wrap-around DC Offset	R			
030	Ch.3 Freq Hi	R/W	090	Ch.2 Wrap-around Frequency High	R	768	Module Design Version[1]	
034	Ch.3 Freq Lo	R/W	094	Ch.2 Wrap-around Frequency Low	R	76C	Module Design Revision[1]	R
038	Ch.3 Phase	R/W	098	Ch.2 Wrap-around Amplitude	R	770	Module DSP[1]	R
03C	Ch.3 Amplitude	R/W	09C	Ch.2 Wrap-around DC Offset	R	774	Module FPGA[1]	R
						778	Module ID	R

Note: 1. Pending

Frequency

Type: 32 bit unsigned integer
Range: 0 – 130,000 (from 1 to 9 Hz, amplitude is functional, but not to accuracy specification)
Read/Write: R/W
Initialized Value: 1000

Frequency High and *Frequency Low* registers combined to determine desired frequency in 1 Hz resolution. LSB is 1 Hz. Frequency is updated on write to Low register. Out-of-range data will be changed to the maximum allowable value. When phase locked, phase is reset when channel 1frequency is changed. If phase is NOT locked, phase remains unchanged when frequency is changed.

FREQUENCY HIGH REGISTER																FREQUENCY LOW REGISTER															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Phase

Type: 16-bit signed integer
Range: ±180 degrees
Read/Write: R/W
Initialized Value: 0

Enter the desired phase offset, relative to channel 1. LSB is approximately 0.088°. When phase locked, phase is reset when channel 1frequency is changed. If phase is NOT locked, phase remains unchanged when frequency is changed. Enter as per formula,

Phase = Register Value / 32768 x 180 Degrees.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PHASE	S	D	D	D	D	D	D	D	D	D	D	D	X	X	X	X	S=SIGN BIT, D=DATA BIT

Amplitude

Type: 16 bit unsigned integer
Range: 0 to 65535 (0 to 10 volts peak E1 ; 0 to 15 volts peak E2)
Read/Write: R/W
Initialized Value: 0

Value determines peak amplitude of selected waveform. Amplitude in combination with the programmed DC Offset cannot be greater that the maximum or full scale output of that module. For module E1, resolution is 10/65536 or approximately 0.15 millivolts. For module E2 resolution is 15/65536 or approximately 0.22 millivolts. From 1 to 9 Hz, amplitude is not accurate. Enter as per formula,

Peak-to-Peak Voltage = 10*Value/65535 Volts Peak, for module E1, (≤ 10 – magnitude of DC Offet).

Peak-to-Peak Voltage = 15*Value/65535 Volts Peak, for module E2, (≤ 15 – magnitude of DC Offet).

Where Volts Peak is half Peak-to-Peak Voltage. Out-of-range data will be changed to the maximum allowable value. From 1 to 9 Hz, amplitude is functional, but not to accuracy specification.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

DC Offset

Type: 16 bit signed integer
Range: -32767 to +32767 (±10 volts E1 ; ±15 volts E2)
Read/Write: R/W
Initialized Value: 0

Value determines DC offset of selected waveform, in 0.30 millivolt resolution.
Enter as per formula,

DC Offset Voltage = 10*Value/32768 Volts DC, for Module E1

DC Offset Voltage = 15*Value/32768 Volts DC, for Module E2

Out-of-range data will be changed to the maximum allowable value.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Mode

Type: binary word
Range: 0, 1, or 2
Read/Write: R/W
Initialized Value: 0 (Sine Wave)

This register is used to select desired waveform using bits D0 and D1. Use bit D2 to enable phase lock function. L=1 to enable, L=0 to disable. When phase lock is enabled, channel 2, 3, and 4 are phase locked to the master signal channel 1. When phased locked, the signal of channels 2, 3 and 4 will be identical to channel 1 in *frequency* and *type* (sine, triangular or square). When phase locked, phase is reset when frequency is changed.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODE and LOCK	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**0**	**0**	SINE WAVE
	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**0**	**1**	TRIANGULAR WAVE
	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**1**	**0**	SQUARE WAVE
	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**1**	**1**	SINE WAVE (same as 00)

Wrap-around Frequency

Type: 32 bit unsigned integer
Range: 0 – 130,000 (from 1 to 9 Hz, amplitude is functional, but not to accuracy specification)
Read/Write: R
Initialized Value: N/A

Read *Wrap-around Frequency High* and *Frequency Low* registers combined to determine desired frequency in 1 Hz resolution. LSB is 1 Hz.

FREQUENCY HIGH REGISTER																	FREQUENCY LOW REGISTER															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

Wrap-around Amplitude

Type: 16 bit unsigned integer
Range: 0 to 65535 (0 to 10 volts peak E1 ; 0 to 15 volts peak E2)
Read/Write: R
Initialized Value: N/A

Read *Wrap-around Amplitude* for D2 BIT test value to verify peak amplitude of selected waveform. For module E1, resolution is 10/65536 or approximately 0.15 millivolts. For module E2 resolution is 15/65536 or approximately 0.22 millivolts. From 1 to 9 Hz, amplitude is not accurate. Decode value as per formula,

Peak-to-Peak Voltage = 10*Value/65535 Volts Peak, for module E1

Peak-to-Peak Voltage = 15*Value/65535 Volts Peak, for module E2

where Volts Peak is half Peak-to-Peak Voltage.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Wrap-around DC Offset

Type: 16 bit signed integer
Range: -32767 to +32767 (±10 volts E1 ; ±15 volts E2)
Read/Write: R
Initialized Value: N/A

Read *Wrap-around DC Offset* for D2 BIT test value to verify DC offset of selected waveform, in 0.30 millivolt resolution. Decode value as per formula,

DC Offset Voltage = 10*Value/32768 Volts DC, for Module E1

DC Offset Voltage = 15*Value/32768 Volts DC, for Module E2

Out-of-range data will be changed to the maximum allowable value.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII “1” in upper byte and ASCII space in lower byte for Module Design Version “1 ” is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN VERSION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “1”								ASCII “ ”								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII “B” in upper byte and ASCII space in lower byte for Module Design Revision “B ” is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “B”								ASCII “ ”								

Module DSP

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4531h

Read register to determine Module ID in ASCII. For example, find ASCII "E" in upper byte and ASCII "1" in lower byte, for Module "E1," together 4531h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "E"								ASCII "1"								

BIT Status

Type: binary word
Range: 0 to 15
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Built-In-Test (BIT) Status. Channel Status Data bit (Chn, where n is 1, 2, 3 or 4) is fail, high true, and indicates that the channel is not operating spec compliant. Passing BIT status indicates that channel Frequency, Amplitude and DC Offset is as programmed. Status is latched. Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time. BIT is operating at all times and cannot be enabled or disabled using the General use *Test Enable* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

BIT Status Interrupt Enable

Type: binary word
Range: 0 to 15
Read/Write: R/W
Initialized Value: 0

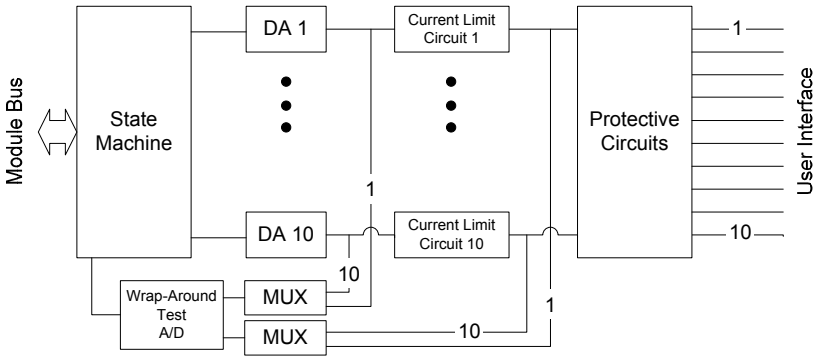
Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 0 to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS INTR ENA	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

D/A (MODULE F OR J)

Ten (10) D/A channels are provided per module and includes extensive diagnostics. Overloaded outputs will be detected, with the results displayed in a status word. This module incorporates major diagnostic capabilities that offer substantial improvements to system reliability because user is alerted to malfunctions within 5 seconds. Two different tests, one off-line (D2) and one on-line (D3) can be selected:

DA Module Block Diagram



The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 0.2% FS and monitored for shorted output. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

The (D3) test uses an internal A/D that measures all D/A channels while they remain connected to the I/O. Each channel will be checked to a test accuracy of 0.2% FS. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from "1" to "0". The test can be stopped at any time. This test requires no user programming and can be enabled or disabled via the bus. **CAUTION:** D/A Outputs are active during this test. Check connected loads for interaction.

D/A Over Current (short circuit) monitoring is disabled during D3 testing.

D/A (F or J) (not J7) MODULE MEMORY MAP

000	Data 1	R/W	028	Polarity 1	R/W	050	Wrap-around 1	R/W	6F8	Test Enable	R/W
004	Data 2	R/W	02C	Polarity 2	R/W	054	Wrap-around 2	R/W	6FC	D2 Verify	R/W
008	Data 3	R/W	030	Polarity 3	R/W	058	Wrap-around 3	R/W			
00C	Data 4	R/W	034	Polarity 4	R/W	05C	Wrap-around 4	R/W	700	BIT Status Ch.1-10	R
010	Data 5	R/W	038	Polarity 5	R/W	060	Wrap-around 5	R/W	704	Over Current Status Ch.1-10	R
014	Data 6	R/W	03C	Polarity 6	R/W	064	Wrap-around 6	R/W	708	BIT Stat Interrupt Enable Ch.1-10	R/W
018	Data 7	R/W	040	Polarity 7	R/W	068	Wrap-around 7	R/W	70C	Over Current Interrupt Enable Ch.1-10	R/W
01C	Data 8	R/W	044	Polarity 8	R/W	06C	Wrap-around 8	R/W			
020	Data 9	R/W	048	Polarity 9	R/W	070	Wrap-around 9	R/W	768	Module Design Version[1]	R
024	Data 10	R./W	04C	Polarity 10	R/W	074	Wrap-around 10	R/W	76C	Module Design Revision[1]	R
									770	Module DSP[1]	R
									774	Module FPGA[1]	R
									778	Module ID	R
									7C0	BIT Interrupt Vector	R/W
									7C4	Over-Current Interrupt Vector	R/W

Note: 1. Pending

Write D/A output

If using bi-polar mode, write 16 bit 2's complement word to the channel's *Data register* (7FFFh=+FS, 8000h=-FS) If using unipolar mode, write 16 bit binary word to the channel's *Data register* (range: 0 to FFFFh=FS).

D/A Output Polarity

Write integer 4 to the channel's *D/A Polarity register* for unipolar mode. Write integer 0 to the channel's *D/A range register* for bi-polar mode.

D/A Wrap-Around

Read D/A *wrap-around data* register, 16 bit 2's complement word (7FFFh=+FS, 8000h=-FS) bipolar mode, or 16 bit binary word (range 0 to FFFFh=FS)

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1"								ASCII " "								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "B"								ASCII " "								

Module DSP

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4E37h

Read register to determine Module ID in ASCII. For example, find ASCII "J" in upper byte and ASCII "7" in lower byte for Module "J7," together 4E37h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "J"								ASCII "7"								

BIT Status

Check the corresponding bit for a channel's BIT Status. A "0" =Normal; "1" = Non-compliant D/A conversion (outside 0.2% FS accuracy spec). Reading any status bit will cause that bit to be unlatched. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status

Check the corresponding bit of the *Over Current Status* registers for over current draw for each active channel. A "0" =Normal; "1" = Over Current. An over current draw from the output of any D/A channel is detected within 2 seconds and will latch the corresponding bit in the *Over Current Status* register. Reading any status bit will cause unlatch the entire register. Over Current Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status	X	X	X	X	X	X	Ch. 10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status Interrupt Enable

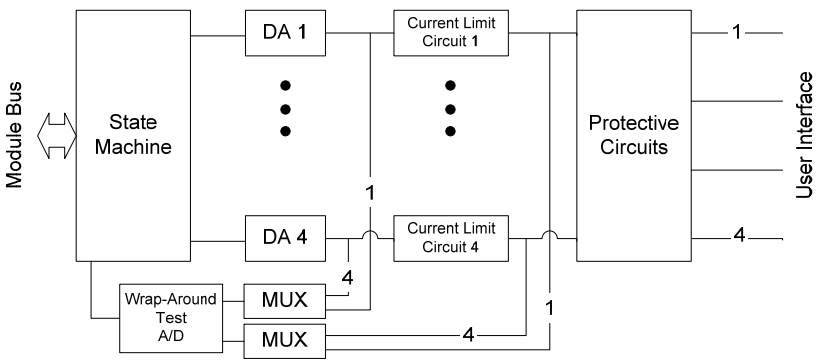
Set the bit to enable interrupts for the corresponding channel monitored for Over Current Status.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status Intr Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

HIGH VOLTAGE D/A (MODULE J7)

Four (4) D/A channels are provided per module and includes extensive diagnostics. To save power, DC-to-DC output drive is internally scaled according to programmed output range. Overloaded outputs will be detected, with the results displayed in a status word. This module incorporates major diagnostic capabilities that offer substantial improvements to system reliability because user is alerted to malfunctions within 5 seconds. Two different tests, one off-line (D2) and one on-line (D3) can be selected:

High Voltage DA Module Block Diagram



The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 2% FS and monitored for shorted output. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

The (D3) test uses an internal A/D that measures all D/A channels while they remain connected to the I/O. Each channel will be checked to a test accuracy of 2% FS. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from "1" to "0". The test can be stopped at any time. This test requires no user programming and can be enabled or disabled via the bus. **CAUTION:** D/A Outputs are active during this test. Check connected loads for interaction.

D/A Over Current (short circuit) monitoring is disabled during D3 testing.

D/A (J7) MODULE MEMORY MAP

000	Data 1	R/W	020	Polarity 3	R/W	1A0	BIT Status Ch.1-4	R
004	Data 2	R/W	024	Polarity 4	R/W	1A8	Over Current Status Ch.1-4	R
008	Data 3	R/W	028	Wrap-around 1	R/W	1C0	BIT Stat Interrupt Enable Ch.1-4	R/W
00C	Data 4	R/W	02C	Wrap-around 2	R/W	1D8	Over Current Interrupt Enable Ch.1-4	R/W
010	Range 1 & 2	R/W	030	Wrap-around 3	R/W			
014	Range 3 & 4	R/W	034	Wrap-around 4	R/W	768	Module Design Version[1]	R
018	Polarity 1	R/W				76C	Module Design Revision[1]	R
01C	Polarity 2	R/W				770	Module DSP[1]	R
						774	Module FGPA[1]	R
						778	Module ID	R
						7C0	BIT Interrupt Vector	R/W
						7C4	Over-Current Interrupt Vector	R/W

Write D/A Output

If using bi-polar mode, write 16 bit 2's complement word to the channel's *Data register* (7FFFh=+FS, 8000h=-FS) If using unipolar mode, write 16 bit binary word to the channel's *Data register* (range: 0 to FFFFh=FS). Because output resolution is 12bits, enter LSBs D0 through D3 as zero. At power-on, output is initialized to 0 volts.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	0	0	0	0	D=DATA BIT

D/A Output Range

Program voltage range for channel pairs (1 & 2, or 3 & 4) from 20 to 80 volts. For 20 volts, enter integer 20. Resolution is 10 volts. 10 ma/channel maximum (source or sink) for up to 80VDC.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
										64	32	16	8	4	2	1	value in volts (LSB=1volt)
RANGE	X	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D=DATA BIT
												1	0	1	0	0	20 volts
												1	1	1	1	0	30 volts
											1	0	1	0	0	0	40 volts
											1	1	0	0	1	0	50 volts
											1	1	1	1	0	0	60 volts
										1	0	0	0	1	1	0	70 volts
										1	0	1	0	0	0	0	80 volts

D/A Output Polarity

Write integer 4 to the channel's *D/A range register* for unipolar mode. Write integer 0 to the channel's *D/A range register* for bi-polar mode.

D/A Wrap-Around

Read D/A *wrap-around data* register, 16 bit 2's complement word (7FFFh=+FS, 8000h=-FS) bipolar mode, or 16 bit binary word (range 0 to FFFFh=FS)

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1"								ASCII " "								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "B"								ASCII " "								

Module DSP

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4A37h

Read register to determine Module ID in ASCII. For example, find ASCII "J" in upper byte and ASCII "1" in lower byte for Module "J7," together 4A37h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "J"								ASCII "7"								

BIT Status

Check the corresponding bit for a channel's BIT Status. A "0" =Normal; "1" = Non-compliant D/A conversion (outside 2% FS accuracy spec). Reading any status bit will cause that bit to be unlatched. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status

Check the corresponding bit of the *Over Current Status* registers for over current draw for each active channel. A "0" =Normal; "1" = Over Current. An over current draw from the output of any D/A channel is detected within 2 seconds and will latch the corresponding bit in the *Over Current Status* register. Reading any status bit will cause unlatch the entire register. Over Current Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

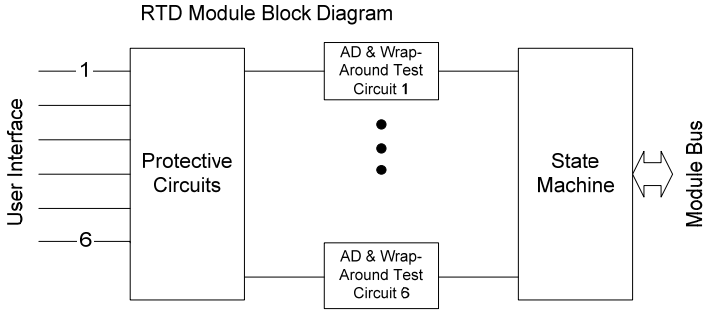
Over Current Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored for Over Current Status.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status Intr Enable	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

RTD (MODULE G4)

The RTD channels use individual A/D converters. All RTD channels are self-calibrating because each channel, on a rotating basis, is automatically calibrated to eliminate offset and gain errors. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution. Open inputs will be detected, with the results displayed in a status word. All inputs are double buffered for immediate availability. External excitation not required.



The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 0.2% FS and monitored for open input. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus.

RTD Open Circuit monitoring is disabled during D3 testing.

RTD (G) MODULE MEMORY MAP

000	Resistance 1	R	018	Range 1	R/W	030	3 or 4 Wire Mode 1[1]	R/W	1A0	BIT Status Ch.1-6	R
004	Resistance 2	R	01C	Range 2	R/W	034	3 or 4 Wire Mode 2[1]	R/W	1A4	Open Status Ch.1-6	R
008	Resistance 3	R	020	Range 3	R/W	038	3 or 4 Wire Mode 3[1]	R/W	1C0	BIT Stat Interrupt Enable Ch.1-6	R/W
00C	Resistance 4	R	024	Range 4	R/W	03C	3 or 4 Wire Mode 4[1]	R/W	1D4	Open Stat INTR Enable Ch.1-6	R/W
010	Resistance 5	R	028	Range 5	R/W	040	3 or 4 Wire Mode 5[1]	R/W			
014	Resistance 6	R	02C	Range 6	R/W	044	3 or 4 Wire Mode 6[1]	R/W	768	Module Design Version	R
									76C	Module Design Revision	R
									770	Module DSP	R
									774	Module FPGA	R
									778	Module ID	R

Note: 1. For 2 or 3 Wire Modes, Consult Factory

Resistance

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Resistance measurement is a binary word and is dependant upon range.
For example, if the 0.01 ohms per count range is selected: 2710h x 0.01 = 10000 x 0.01 = 100 ohms.

The resistance/temperature relationship varies among RTDs and is function of its composite material (ex, Platinum, Copper, Nickel-Iron, Nickel, etc). An RTD's "Alpha" Temperature Coefficient and its nominal resistance (at say 0°C), while operating within its applicable resistance range, provide for a first order approximation.

For best accuracy, use resistance/temperature relationship provided by the RTD manufacture:

Select associated *Range* (0-655, or 1-2000)
Read *Resistance* and scale accordingly (0.01 Ω / bit , or 0.03 Ω / bit.)

Calculate temperature using RTD manufacture provided resistance/temperature relationship (a quadratic equation).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESISTANCE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Range

Type: 16 bit unsigned integer
Range: 0 or 1
Read/Write: R/W
Initialized Value: 0

Write “0” for a 0-655 ohm output range, 0.01 Ω / bit.
Write “1” for a 1-2000 ohm output range, 0.03 Ω / bit.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RANGE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

3 or 4 Wire Mode

Consult Factory.

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII “1” in upper byte and ASCII space in lower byte for Module Design Version “1 ” is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “1”								ASCII “ ”								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII “B” in upper byte and ASCII space in lower byte for Module Design Revision “B ” is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “B”								ASCII “ ”								

Module DSP

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Read register to determine Module ID in ASCII. For example, find ASCII “G” in upper byte and ASCII “1” in lower byte for Module “G1,” together 4731h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “G”								ASCII “1”								

BIT Status

Check the corresponding bit for a channel’s BIT Status. A “0” =Normal; “1” = Non-compliant A/D conversion (outside 0.2% FS accuracy spec). Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status

Check the corresponding bit of the *Open Status* registers for open/disconnected RTD for each active channel. A “0” =Normal; “1” = Open (detected after 2 seconds). Reading any status bit will cause that bit to be unlatched. Open Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status	X	X	X	X	X	X	Ch. 10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status Interrupt Enable

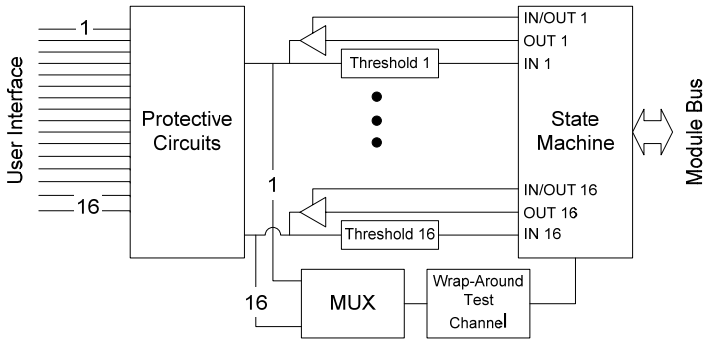
Set the bit to enable interrupts for the corresponding channel monitored for Open Status.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

I/O DISCRETE (MODULE K6)

Discrete (LSI) channels are programmable for either Input or Output. When programmed for Input, they can be used for either voltage or contact sensing. Channels set for contact sensing can be programmed for either pull-up or pull-down. Our unique design eliminates the need for pull-up resistors or mechanical jumpers. Instead, we offer a current source (in groups of 4) that user programs to a desired current level. When programmed for Output, each channel can be set for either High-side, Lo-side or Push-Pull operation. The Modules add diode clamping (useful for inductive loads, such as relays) and thermal protection. The Module is signal and power isolated from the PCI bus. There are 4 user provided Vcc inputs for each 16 channel module. There is one Vcc input for each four channel bank. Vcc must be wired for proper output operation and input operation requiring a "pull-up configuration.

Discrete IO Module Block Diagram



DISCRETE (K) MODULE MEMORY MAP

000	Write Output	Ch.01-16	R/W	098	Upper Threshold	Ch.08	R/W	130	De-bounce time	Ch.15	R/W
004	Read I/O	Ch.01-16	R	09C	Lower Threshold	Ch.08	R/W	134	Max High Threshold	Ch.16	R/W
008	Max High Threshold	Ch.01	R/W	0A0	Min Low Threshold	Ch.08	R/W	138	Upper Threshold	Ch.16	R/W
00C	Upper Threshold	Ch.01	R/W	0A4	De-bounce time	Ch.08	R/W	13C	Lower Threshold	Ch.16	R/W
010	Lower Threshold	Ch.01	R/W	0A8	Max High Threshold	Ch.09	R/W	140	Min Low Threshold	Ch.16	R/W
014	Min Low Threshold	Ch.01	R/W	0AC	Upper Threshold	Ch.09	R/W	144	De-bounce time	Ch.16	R/W
018	De-bounce time	Ch.01	R/W	0B0	Lower Threshold	Ch.09	R/W	148	Input/Output Format	Ch.01-08	R/W
01C	Max High Threshold	Ch.02	R/W	0B4	Min Low Threshold	Ch.09	R/W	14C	Input/Output Format	Ch.09-16	R/W
020	Upper Threshold	Ch.02	R/W	0B8	De-bounce time	Ch.09	R/W	150	Current For Sink/Source, Bank 1	Ch.01-04	R/W
024	Lower Threshold	Ch.02	R/W	0BC	Max High Threshold	Ch.10	R/W	154	Current For Sink/Source, Bank 2	Ch.05-08	R/W
028	Min Low Threshold	Ch.02	R/W	0C0	Upper Threshold	Ch.10	R/W	158	Current For Sink/Source, Bank 3	Ch.09-12	R/W
02C	De-bounce time	Ch.02	R/W	0C4	Lower Threshold	Ch.10	R/W	15C	Current For Sink/Source, Bank 4	Ch.13-16	R/W
030	Max High Threshold	Ch.03	R/W	0C8	Min Low Threshold	Ch.10	R/W	160	Pull Up/Down Current Config	Ch.01-16	R/W
034	Upper Threshold	Ch.03	R/W	0CC	De-bounce time	Ch.10	R/W	168	Vcc Value, Bank 1	Ch.01-04	R
038	Lower Threshold	Ch.03	R/W	0D0	Max High Threshold	Ch.11	R/W	16C	Vcc Value, Bank 2	Ch.05-08	R
03C	Min Low Threshold	Ch.03	R/W	0D4	Upper Threshold	Ch.11	R/W	170	Vcc Value, Bank 3	Ch.09-12	R
040	De-bounce time	Ch.03	R/W	0D8	Lower Threshold	Ch.11	R/W	174	Vcc Value, Bank 4	Ch.13-16	R
044	Max High Threshold	Ch.04	R/W	0DC	Min Low Threshold	Ch.11	R/W	178	Reset Over-Current	Ch.01-16	R/W
048	Upper Threshold	Ch.04	R/W	0E0	De-bounce time	Ch.11	R/W				
04C	Lower Threshold	Ch.04	R/W	0E4	Max High Threshold	Ch.12	R/W	1A0	Status Fault	Ch.01-16	R
050	Min Low Threshold	Ch.04	R/W	0E8	Upper Threshold	Ch.12	R/W	1A8	Status Over-Current	Ch.01-16	R
054	De-bounce time	Ch.04	R/W	0EC	Lower Threshold	Ch.12	R/W	1AC	Status Max Hi Threshold	Ch.01-16	R
058	Max High Threshold	Ch.05	R/W	0F0	Min Low Threshold	Ch.12	R/W	1B0	Status Min Lo Threshold	Ch.01-16	R
05C	Upper Threshold	Ch.05	R/W	0F4	De-bounce time	Ch.12	R/W	1B4	Status Mid Range	Ch.01-16	R
060	Lower Threshold	Ch.05	R/W	0F8	Max High Threshold	Ch.13	R/W	1B8	Status Lo-Hi Transition	Ch.01-16	R
064	Min Low Threshold	Ch.05	R/W	0FC	Upper Threshold	Ch.13	R/W	1BC	Status Hi-Lo Transition	Ch.01-16	R
068	De-bounce time	Ch.05	R/W	100	Lower Threshold	Ch.13	R/W	1C0	Interrupt Fault Enable	Ch.01-16	R/W
06C	Max High Threshold	Ch.06	R/W	104	Min Low Threshold	Ch.13	R/W	1D8	Interrupt Over-Current Enable	Ch.01-16	R/W
070	Upper Threshold	Ch.06	R/W	108	De-bounce time	Ch.13	R/W	1DC	Interrupt Max Hi Threshold Enable	Ch.01-16	R/W
074	Lower Threshold	Ch.06	R/W	10C	Max High Threshold	Ch.14	R/W	1E0	Interrupt Min Lo Threshold Enable	Ch.01-16	R/W
078	Min Low Threshold	Ch.06	R/W	110	Upper Threshold	Ch.14	R/W	1E4	Interrupt Mid-Range Fault Enable	Ch.01-16	R/W
07C	De-bounce time	Ch.06	R/W	114	Lower Threshold	Ch.14	R/W	1E8	Interrupt Lo-Hi Transition Enable	Ch.01-16	R/W
080	Max High Threshold	Ch.07	R/W	118	Min Low Threshold	Ch.14	R/W	1EC	Interrupt Hi-Lo Transition Enable	Ch.01-16	R/w
084	Upper Threshold	Ch.07	R/W	11C	De-bounce time	Ch.14	R/W				
088	Lower Threshold	Ch.07	R/W	120	Max High Threshold	Ch.15	R/W	768	Module Design Version		R
08C	Min Low Threshold	Ch.07	R/W	124	Upper Threshold	Ch.15	R/W	76C	Module Design Revision		R
090	De-bounce time	Ch.07	R/W	128	Lower Threshold	Ch.15	R/W	770	Module DSP		R
094	Max High Threshold	Ch.08	R/W	12C	Min Low Threshold	Ch.15	R/W	774	Module FPGA		R
								778	Module ID		R

Write Output

When a channel is configured for Output, write logic level High (“1”) or Low (“0”) to associated channel bit, in 16 bit binary word. Each bit corresponds to one of 16 channels (See Register Bit Map.) Output logic is defined by the provided Vcc voltage to that channel bank. There are four channels per bank (See J1 & J2, or P2 & P0 pin out.)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Read I/O

Independent of channel configuration (Input or Output), read logic state High (“1”) or Low (“0”) as defined by channel threshold values. Each bit of 16-bit binary word corresponds to one of 16 channels.

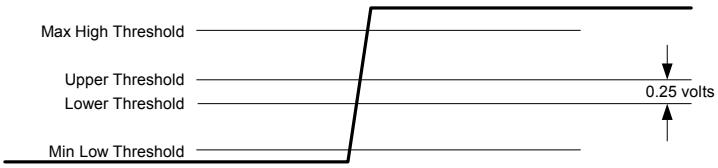
REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Threshold Programming

All four threshold levels must be programmed. For Input, threshold levels define logic. For output, threshold levels are used in BIT (wrap around) test signal monitoring. For proper operation, the threshold values should be programmed such that Max High > Upper > Lower > Min Low Threshold.

For proper operation, all four voltage thresholds must be set in this order:

Max High Threshold
> Upper Threshold
> Lower Threshold
> Min Low Threshold

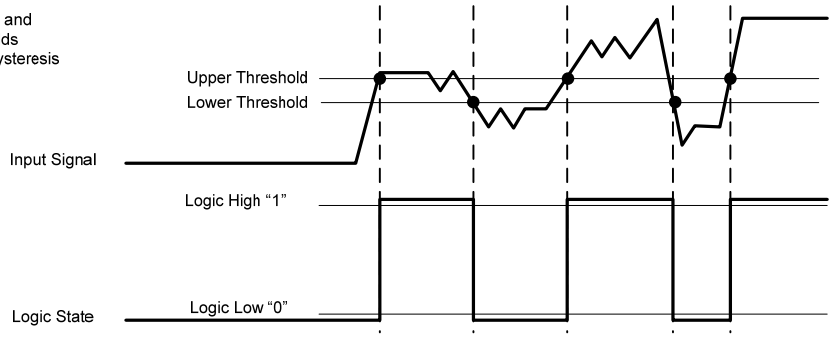


For hysteresis configuration, a 0.25 volt minimum differential between Upper Threshold and Lower Threshold is recommended.

Hysteresis

Program Upper and Lower Thresholds to implement the required hysteresis and then add de-bounce time as required. When the input signal exceeds the Upper Threshold, a logic high “1” is maintained until the input signal falls below the Lower Threshold. Conversely, when the input signal falls below the Lower Threshold, a logic low “0” is maintained until the input signal rises above the Upper Threshold. A 0.25 volt minimum differential is recommended between the Upper and Lower Threshold values.

Program Upper and Lower Thresholds to implement hysteresis



When the input signal exceeds the Upper Threshold, a logic high “1” is maintained until the input signal falls below the Lower Threshold. Conversely, the same is true as the signal changes from low to high, or high to low.

Max High Threshold

Maximum High Threshold is programmable per channel from 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv. Assumes that the programmed level is the minimum voltage used to indicate a Max HighThreshold. If a signal is greater then the Max High Threshold value, flag is set in the *Max High Threshold Status register*. The Max High Threshold register may be used to monitor any type of high signal voltage condition or threshold such as a “Short to +V” as it applies to input measurement as well as contact sensing applications.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
MAX HIGH THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

Upper Threshold

Upper Threshold is programmable per channel from 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv. A signal is considered logic High (“1”) when its value exceeds the Upper threshold and does not consequently fall below the Lower threshold in less than the programmed De-bounce time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
UPPER THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

Lower Threshold

Lower Threshold is programmable per channel from 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv. A signal is considered logic Low (“0”) when its value falls below the Lower threshold and does not consequently rise above the Upper Threshold in less than the programmed De-bounce time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
LOWER THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

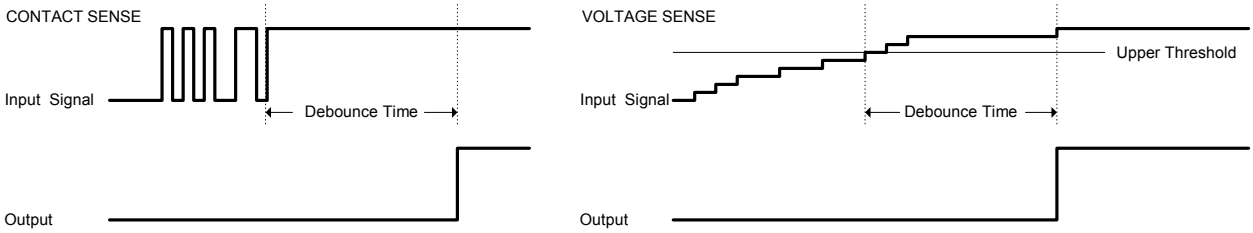
Min Low Threshold

Minimum Low Threshold is programmable per channel 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv**.** Assumes that the programmed level is the maximum voltage used to indicate a Min Low Threshold. If a signal is less then the Min Low Threshold value, a flag is set in the *Min Low Threshold Status register*. The Min Low Threshold register may be used to monitor any type of low signal voltage condition or threshold such as a “Short to Ground” as it applies to input measurement as well as contact sensing applications.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
MIN LOW THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

De-bounce time

Enter required de-bounce time into appropriate channel registers. Enter time in 20μs increments, up to 0.655 seconds. LSB= 20 μs. Value is 15 bits (MSB=don’t care). De-bounce defaults to 0 upon reset. For contact sensing, De-bounce time is much like a glitch filter. Signal pulse widths less than the De-bounce time are filtered or ignored. Once a signal level is stable for a period longer than the De-bounce time (see Upper and Lower Threshold described above), a logic transition is validated. For voltage sensing, the input signal level must exceed its associated threshold for a time greater then the De-bounce time for the logic transition to be validated (see Upper and Lower Threshold described above). Once valid, the interrupt transition register channel flag is set and the output logic changes state. Enter a value of 0 to disable De-bounce filtering.



REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
		~328	~164	~82	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	value in mSec (LSB=20μS)
DE-BOUNCE TIME	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

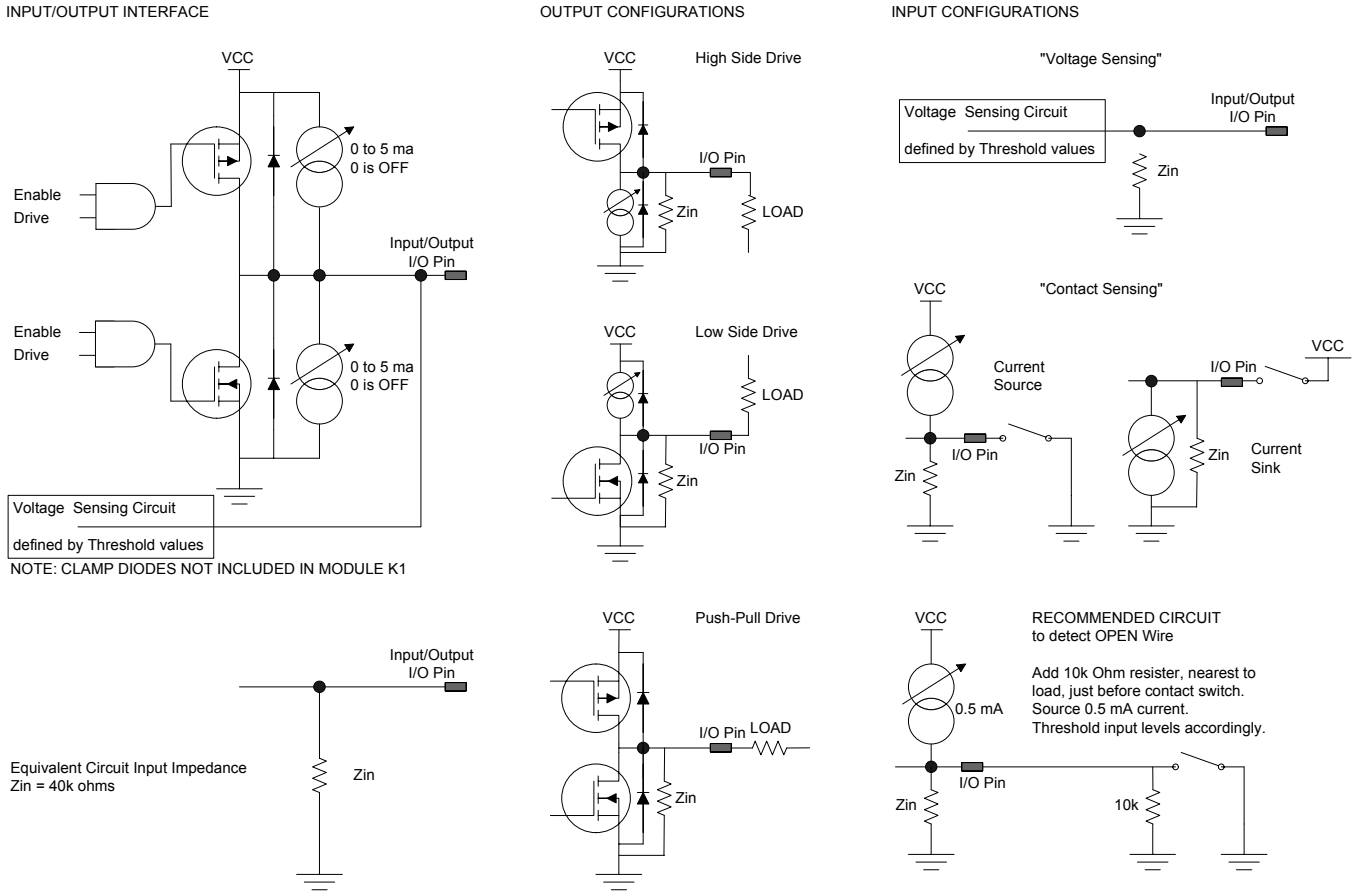
Input/Output Interface

The Input/Output (I/O) Interface can be configured in a variety of ways. A pair of drive FETs and current circuits are provided at each I/O pin. See I/O interface diagram below.

Output: When configured as an output, the interface can act as a "High-Side", "Low-Side" or "Push-Pull" drive, providing up to 500ma per channel. The total output per module (16 channels) cannot exceed 2 amps.

Input: When configured as an input, output drivers are disabled. I/O interface can act as a current source, current sink or voltage sensing circuit. For contact sensing, set each channel for pull-up or pull-down using the *Pull-Up/Down Current Configuration* register and enter the appropriate current level in the *Current For Sink/Source* register. Define contact closure and hysteresis using Upper and Lower Threshold. See *Read I/O* register to read input signal logic state. *No additional resistors or hardware is required to provide for current flow.* A current value of zero disables the current source/sink circuits and configures for voltage sensing. Default is voltage sensing.

All four threshold levels must be programmed. For input, threshold levels define logic state. For output, threshold levels are used in BIT test (wrap-around) signal monitoring.



To detect an OPEN line when **contact sensing,** add 10k ohm resistor R_{nl} nearest to load. Program open detect current I_{od} and calculate open contact condition, drop voltage V_{open} at I/O pin. Select sourcing current I_{od} such that drop voltage ΔV is about 80% of Vcc. If open detect resistance R_{od} is the parallel combination of the near load resistance R_{nl} and the circuit input impedance Z_{in}. Then

$R_{od} = R_{nl} \,||\, Z_{in} = 10k \,||\, 40k = 8k.$

If user provided Vcc is 10v,

$I_{od} = 0.8\ Vcc / R_{od} = 0.8 \times 10 / 8k = 1ma.$

If I_{od} = 1ma, we get open contact condition, drop voltage V_{open} at the I/O pin,

$V_{open} = I_{od}R_{od} = 1ma \times 8k\Omega = 8.0$ volts.

If load is current sink, Program Maximum Upper Threshold T_{mu}, some 20% greater then V_{open} , maintaining

$Vcc > T_{mu} > V_{open} > T_{ut}$,

T_{mu} $= 1.2\ V_{open}$ $= 1.2 \times 8$ $= 9.6$ volts.

Program Upper Threshold T_{ut} 20% less then V_{open}

$T_{ut} = 0.8\ V_{open}$ $= 0.8 \times 8$ $= 6.4$ volts.

Accordingly, program Lower Threshold T_{lt} at 20% Vcc and Minimum Lower Threshold T_{ml} at 10% Vcc

$T_{lt} = 0.2\ Vcc$ $= 0.2 \times 10$ $= 2$ volts.

$T_{ml} = 0.1\ Vcc$ $= 0.1 \times 10$ $= 1$ volts.

To detect a line SHORT when **contact sensing** and continuing with this example, user needs to add series resistance nearest to load, Rs and calculate closed contact condition, drop voltage V_{closed} at I/O pin. Resistance nearest to load, R_s should be negligible as compared to the near load resistance R_{nl} but at least a magnitude greater than any resistance due to wire length. A value of 150 ohms would be appropriate for Rs. Then

$V_{closed} = I_{od}R_s$ $= 1ma \times 0.1k\Omega$ $= 0.15$ volts.

Program Lower Threshold T_{mu}, greater then V_{closed} maintaining

$Vcc >> T_{lt} > V_{closed} > T_{ml} > 0$

$T_{lt} > 1.2\ V_{closed}$ $> 1.2 \times 0.1$ $= 0.2$ volts.

Program Minimum Lower Threshold T_{ut} 20% less then V_{open}

$T_{ml} < 0.8\ V_{closed}$ $< 0.8 \times 0.15$ $= 0.1$ volts.

In general,

$Vcc > T_{mu} > V_{open} > T_{ut}, > T_{lt} > V_{closed} > T_{ml} > 0$, $T_{ut} - T_{lt} \geq 0.25mV$ for hysteresis configuration

To detect a Short to Vcc, Program Maximum Upper Threshold T_{mu}, where

$Vcc > T_{mu} > V_{loadmax}$, where $V_{loadmax}$ is the maximum voltage potential on the I/O pin.

To detect a Short to Ground, Program Minimum Lower Threshold T_{ml}, where

$Vcc > > V_{loadmin} > T_{ml}$, where $V_{loadmin}$ is the minimum voltage potential on the I/O pin.

Consider the following programming options:

Output Programming Examples:

Figure	INPUT/OUTPUT FORMAT 2 bits per channel	Integer	PULL-UP/DOWN Configuration 1 bit per 4-channel bank	Integer	CURRENT FOR SOURCE/SINK One register per 4-channel bank	Integer
1	Output Ch1, High Side Drive	2	without current pull down	X	NO current source	0
1	Output Ch1-4, High Side Drive	170	Ch1-4 with current pull down[1]	14	1 ma	10
1	Output Ch5-8, High Side Drive	43520	Ch5-8 with current pull down[1]	13	2 ma	20
1	Output Ch1-8, High Side Drive	43690	Ch1-8 with current pull down[1]	12	2 ma	20
2	Output Ch1, Low Side Drive	1	without current pull up	X	NO current source	0
2	Output Ch1-4, Low Side Drive	85	Ch1-4 with current pull up[1]	1	1 ma	10
2	Output Ch1-8, Low Side Drive	21845	Ch1-8 with current pull up[1]	3	2 ma	20
3	Output Ch1, Push-Pull	3	Not Applicable – DON'T CARE	X	Not Applicable – DON'T CARE	X

Note 1: Use current source for Wired-OR or other related applications.

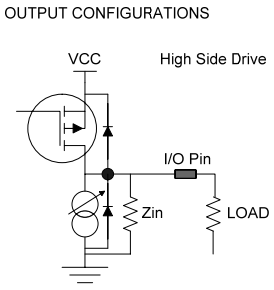


Figure 1

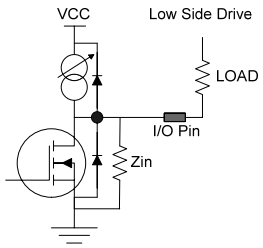


Figure 2

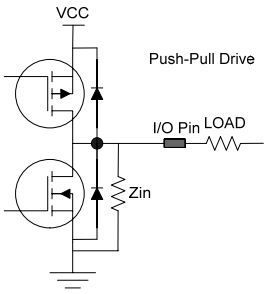


Figure 3

Input Programming Examples:

Figure	INPUT/OUTPUT FORMAT 2 bits per channel	Integer	PULL-UP/DOWN Configuration 1 bit per 4-channel bank	Integer	CURRENT FOR SOURCE/SINK One register per 4-channel bank	Integer
4	Input Ch1-8, voltage sensing (default)	0	without current source/sink	X	NO current source (default)	0
5	Input Ch1-8, contact sensing	0	Ch1-8 with current pull up	3	1 ma	10
6	Input Ch1-8, contact sensing	0	Ch1-8 with current pull down	12	2 ma	20
7	Input Ch1-8, OPEN line detect, load is current sink	0	Ch1-8 with current pull up	3	0.5 ma Program Max Upper Threshold[2]	5
6[1]	Input Ch1-8, OPEN line detect, load is current source	0	Ch1-8 with current pull down	12	0.5 ma Program Min Lower Threshold[3]	5

Notes 1. Figure 6 with 10k ohm resistor nearest load (as in figure 7)

2. $Vcc > T_{mu} > I_{od}R_{od}$, where load is current sinking

3. $T_{ml} < Vcc - I_{od}R_{od}$, where load is current sourcing

INPUT CONFIGURATIONS

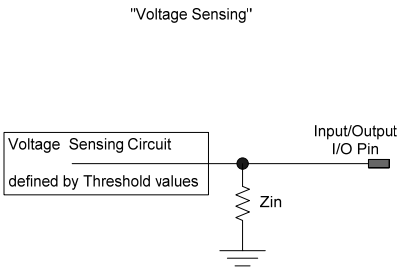


Figure 4

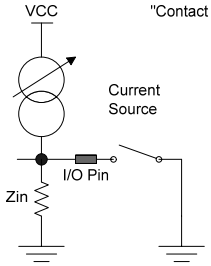


Figure 5

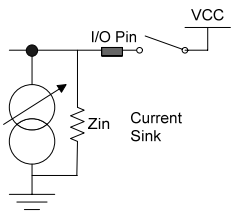


Figure 6

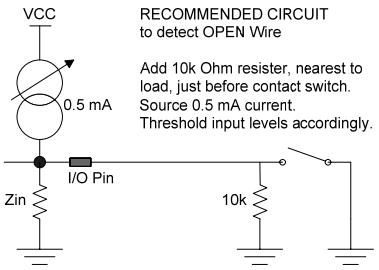


Figure 7

Current for Source/Sink

Program any current from 0 to 5 ma. Programs entire bank; there are 4 channels per bank. For 5ma, enter integer 50. Resolution is 100µa per bit (LSB=100µa). A current value of zero disables the current source/sink circuits and configures for voltage sensing.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
											3.2	1.6	0.8	0.4	0.2	0.1	value in mA (LSB=100µA)
CURRENT	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input/Output format

Configure channels in groups of 8. Write integer 0 for input, 1, 2 or 3 for output. While each channel may be programmed for either input or output individually, Pull-up/down Current Configuration must be programmed in four channel banks.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INPUT/OUTPUT CH 01-08	Ch.08		Ch.07		Ch.06		Ch.05		Ch.04		Ch.03		Ch.02		Ch.01		Channel
INPUT/OUTPUT CH 09-16	Ch.16		Ch.15		Ch.14		Ch.13		Ch.12		Ch.11		Ch.10		Ch.09		Channel
INPUT/OUTPUT	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT

Integer	D_H	D_L	
0	**0**	**0**	Input
1	**0**	**1**	Output, Low-side switched, with/without current pull up
2	**1**	**0**	Output, High-side switched, with/without current pull down
3	**1**	**1**	Output, push-pull

Pull-up/down Current Configuration

Set bit "1"=to configure Bank to Pull-up, or clear bit "0" to configure Bank to Pull-down. Each data bit configures entire bank of 4 channels. Defaults to "1"; pull-up configuration. Register data bits D4 through D15 are "don't care": XXXX XXXX XXXX $D_3D_2D_1D_0$

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
VCC VALUE	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	1=Pull-Up, 0=Pull-Down
D0 configures bank 1, channels 1-4 of that module.																**D**	Configure Ch.01-04
D1 configures bank 2, channels 5-8 of that module.															**D**		Configure Ch.05-08
D2 configures bank 3, channels 9-12 of that module.														**D**			Configure Ch.09-12
D3 configures bank 4, channels 13-16 of that module.													**D**				Configure Ch.13-16

Examples: Register value is integer:

Register Value	Data Bits			Channel Configuration, Module 1		
	D15-D2	**D1**	**D0**	Ch. 9-16	Ch. 5-8	Ch. 1-4
0	**0000 0000 0000 00 - -**	**0**	**0**	Pull-Down	Pull-Down	Pull-Down
1	**0000 0000 0000 00 - -**	**0**	**1**	Pull- Down	Pull-Down	Pull-Up
2	**0000 0000 0000 00 - -**	**1**	**0**	Pull- Down	Pull-Up	Pull-Down
3	**0000 0000 0000 00 - -**	**1**	**1**	Pull- Down	Pull-Up	Pull-Up

Vcc Value

Read Vcc voltage at input pin per four channel bank. Value is binary 10 bit word, where LSB=100 mv. Whether configured for input or output, user provided Vcc must be wired for proper operation.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1	value in volts (LSB=100mv)
VCC VALUE	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Reset Over-Current

Write integer "1" to reset all sixteen channels (per module). This register is used to reset disabled channel(s) set to tri-state following an over-current condition. When reset process is complete, processor will write a "0" back to the *Reset Over-Current* register. Card will respond to a Reset command after one second.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESET OVER-CURRENT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	D=DATA BIT

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4B31h

Read register to determine Module ID in ASCII. For example, find ASCII “K” in upper byte and ASCII “1” in lower byte for Module “K1,” together 4B31h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “K”								ASCII “1”								

Automatic background BIT testing

BIT is always enabled and continually checks that each channel is functional. This capability is accomplished by an additional Test A/D that is incorporated into each 16 channel module. The Test A/D is sequentially connected across each channel and compared against the operational channel. Depending upon configuration, the Input data read or Output logic write of the operational channel and Test A/D must agree or a fault is indicated with the results available in the associated status register. Additional testing is provided to check for Over-current condition. *All four threshold levels must be set for each Input or Output channel to validate BIT testing*. The card will write 55h to the *Test (D2) Register*, every 30 seconds. User can periodically clear the *Test (D2) Register* by writing 00h, waiting 30 seconds then reading the register again to verify that background BIT testing is functioning. Testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and associated status register(s) can be checked or polled at any given time. Enable Interrupts, within any interrupt enable register, by setting the appropriate channel bits to 1.

Status indications

Fault – Channel processing (data read or write logic) is inconsistent with redundant test circuit. Status (bit is set) is indicated within 15 seconds. A fault is latched until read. (Testing takes approx. 1 second per channel)

Over-current – If over-current or overload condition is sensed, status is indicated (bit is set) within 80µs.
Max High Threshold – If the signal exceeds this threshold, status is indicated (bit is set) within 40µs.
Min Low Threshold – If the signal falls below this threshold, status is indicated (bit is set) within 40µs.
Lo-Hi Transition – If a Lo to High transition is sensed, status is indicated (bit is set) within 40µs.
Hi-Low Transition – If a High to Low transition is sensed, status is indicated (bit is set) within 40µs.
Mid-Range – When the signal is in-between the Upper and Lower thresholds, status is indicated (bit set) within 40µs.

When status is “indicated,” or bit is “set,” bit value is logic “1.” Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Max Hi Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Min Lo Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Mid-Range	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Max Hi Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Min Lo Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Mid-Range Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

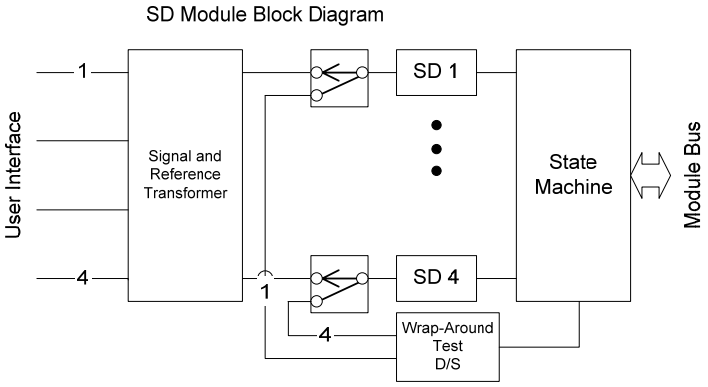
Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored.

When status is “indicated,” or bit is “set,” bit value is logic “1.” Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Max Hi Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Min Lo Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Mid-Range	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Max Hi Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Min Lo Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Mid-Range Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

S/D (MODULE S*)



This S/D measurement design has the capability to automatically shift to higher bandwidths when high acceleration events are encountered. There is not data latency. The shifting is smooth and continuous with no glitches. Tracking rates are only limited to bandwidth restrictions, up to 150 RPS, at 16-bit resolution. Both a software and hardware LATCH feature is provided to permit the user to read all channels at the same time. Reading will unlatch that channel. The angle alert monitors each channel for the programmed angle difference and sets an interrupt as soon as that threshold is reached. Thus, no polling of the angle registers is required until an angle has reached the specified difference. The use of Type II servo loop processing techniques enables tracking, at full accuracy, up to the specified rate. A step input will not cause any hang-up condition. Intermediate transparent latches, on all angle and velocity outputs, assure that valid data is always available. Our synthetic reference compensates for ±60° phase shifts, thus eliminating the need for individual compensation networks.

The (D2) Test initiates automatic background BIT testing. Each channel is checked every 5° to a testing accuracy of 0.05° and each Signal and Reference is always monitored. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled via the bus.

The (D3) Test initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. Results can be read from registers and external reference is not required. Any failure triggers an Interrupt (if enabled). The testing requires no external programming, and can be initiated or stopped via the bus.

The (D0) Test is used to check the card and the PCI interface. All channels are disconnected from the outside world, allowing the user to write any number of input angles to the card and then to read the data from the interface. External reference is not required.

S/D MEMORY MAP

000	SD1 Data Lo	R	07C	SD SYN/RSL SELECT	R/W	100	SD1 Signal Loss Threshold	W/R
004	SD1 Data Hi	R	080	SD1 Angle Δ	R/W	104	SD2 Signal Loss Threshold	W/R
008	SD2 Data Lo	R	084	SD2 Angle Δ	R/W	108	SD3 Signal Loss Threshold	W/R
00C	SD2 Data Hi	R	088	SD3 Angle Δ	R/W	10C	SD4 Signal Loss Threshold	W/R
010	SD3 Data Lo	R	08C	SD4 Angle Δ	R/W	110	SD1 REF Loss Threshold	W/R
014	SD3 Data Hi	R	090	Angle Δ INIT	R/W	114	SD2 REF Loss Threshold	W/R
018	SD4 Data Lo	R	0A0	SD1 Frequency LO	R	118	SD3 REF Loss Threshold	W/R
01C	SD4 Data Hi	R	0A4	SD1 Frequency HI	R	11C	SD4 REF Loss Threshold	W/R
020	SD1 VEL Lo	R	0A8	SD2 Frequency LO	R	120	SD1 VEL SCALE	W/R
024	SD1 VEL HI	R	0AC	SD2 Frequency HI	R	124	SD2 VEL SCALE	W/R
028	SD2 VEL Lo	R	0B0	SD3 Frequency LO	R	128	SD3 VEL SCALE	W/R
02C	SD2 VEL HI	R	0B4	SD3 Frequency HI	R	12C	SD4 VEL SCALE	W/R
030	SD3 VEL Lo	R	0B8	SD4 Frequency LO	R	13C	SIG Status Ch.1-4	R
034	SD3 VEL HI	R	0BC	SD4 Frequency HI	R	140	REF Status Ch.1-4	R
038	SD4 VEL Lo	R	0C0	SD1 VLL	R	144	BIT Status Ch.1-4	R
03C	SD4 VEL HI	R	0C4	SD2 VLL	R	148	SD Lock Status Ch.1-4	R
040	SD1 Bandwidth	R/W	0C8	SD3 VLL	R	14C	SD Angle Δ Status Ch.1-4	R
044	SD2 Bandwidth	R/W	0CC	SD4 VLL	R	150	SIG Status Interrupt Enable Ch.1-4	R/W
048	SD3 Bandwidth	R/W	0D0	SD1 REF	R	154	REF Status Interrupt Enable Ch.1-4	R/W
04C	SD4 Bandwidth	R/W	0D4	SD2 REF	R	158	BIT Status Interrupt Enable Ch.1-4	R/W
050	Bandwidth Select	R/W	0D8	SD3 REF	R	15C	SD Lock Status Interrupt Enable Ch.1-4	R/W
054	SD Ratio 1/2	R/W	0DC	SD4 REF	R	160	SD Angle Δ Interrupt Enable Ch.1-4	R/W
058	SD Ratio 3/4	R/W	0E0	SD1 Encoder Resolution	W/R	200	OSC Freq Lo	W/R
05C	SD Active Channels	R/W	0E4	SD2 Encoder Resolution	W/R	204	OSC Freq HI	W/R
060	SD Track / Hold	R/W	0E8	SD3 Encoder Resolution	W/R	208	OSC Volt Lo	W/R
064	D2 Test Verify	R/W	0EC	SD4 Encoder Resolution	W/R	20C	OSC Volt Hi	W/R
068	Test Enable	R/W						
06C	Test Angle	R/W						
400	Vector Signal Loss	W/R				768	Module Design Version	
404	Vector REF Loss	W/R				770	Module DSP Rev	W/R
408	Vector BIT Fail	W/R				774	Module FPGA Rev	W/R
40C	Vector Lock Loss	W/R				778	Module ID	R
410	Vector Angle Δ	W/R				76C	Module Design Revision	

(S/D data buffering pending)

Data

Date Hi Type: 16 bit unsigned integer
Date Hi & Lo Type: 24 bit unsigned integer (Multi-Speed Applications)
Range: 0 to 359.9945 degrees
Read/Write: R

For Single Speed (Ratio=1) applications, read *Data High* register of that channel. For Multi-Speed applications, read *Data High* register of the even channel (2 or 4) for that pair where 16-bit resolution is required. LSB is approximately 0.0055 degrees.

For better than 16-bit resolution Multi-Speed requirements, use *Data High* and *Data Low* registers combined to determine measured angle with up to 24-bit resolution. First read *Data High* word, then *Data Low* word. Data high word, when read, latches low word. Data Low word, when read, unlatches data. LSB is dependant upon Ratio. A gear ratio of 256 provides for a 24-bit resolution, a ratio of 128 provides for a 23-bit resolution, and so on.. The N-speed information (Multi-Speed, Fine) from the synchro should be connected to the even channel of that pair. The pairs are defined as Ch.1 & 2 and Ch.3 & 4. NOTE: Per bit angle values in below table are approximate.

DATA HIGH REGISTER																DATA LOW REGISTER															
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	X	X	X	X	X	X	X	X

Velocity

Type: 16 bit 2's complement word
Range: 0x7FFF maximum CW rotation to 0x8000 maximum CCW
Read/Write: R
Initialized Value: N/A

Read Velocity Registers of each channel as a 2's complement word, with 7FFFh being maximum CW rotation, and 8000h being maximum CCW rotation.

When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CW would be read as 0863h.
When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CCW would be read as F79Ch.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CW would be read as 192Ah.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CCW would be read as E6D5h.

To convert a velocity word to RPS: **Velocity in RPS = Maximum x Output / Full Scale**

If Velocity Output were E6D5h, and maximum velocity were 50.8626 RPS, then

Velocity in RPS = 50.8626 x E6D5h / 32,768 = 50.8626 x -6,442 / 32,768 = -10 RPS

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
VELOCITY	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT, 2's Complement

Ratio

Type: 16 bit unsigned integer
Range: 1 to 255
Read/Write: R/W
Initialized Value: 1 (Single-Speed)

Enter the desired ratio, as an integer number, in the *Ratio* Register corresponding to the pair of channels to be used for a two-speed, or multi-speed configuration. Example, 36:1 = integer 36. Default is for single speed applications where Ratio = 1.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RATIO	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Angle Δ

Type: 16-bit unsigned integer
Range: 0.05 to 180 degrees
Read/Write: R/W
Initialized Value: 0

Enter the minimum differential angle to associated channel *Angle Δ* register required to trigger an angle change alert. See *Angle Δ Alert* register description for details. MSB=180°; minimum differential is 0.05°.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	approximate value
ANGLE Δ	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Degrees)

Angle Δ Initiate

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Set the bit corresponding to each channel to be monitored for angle change alert. Set bit to "1" for monitoring channels and clear bit to "0" for those not used.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE INTIATE	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL ENABLE BIT

Active Channels

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Set the bit corresponding to each channel to be monitored during BIT testing in the *Active Channel* register. Set bit to "1" for active channels and clear bit to "0" for those not used. Omitting this step will produce false alarms, because unused channels will set faults.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ACTIVE CHANNEL	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL ENABLE BIT

Latch

Type: 16 bit unsigned integer
Range: 0 or 2
Read/Write: R
Initialized Value: 0

Writing the integer 2 to the *Latch* register will cause all the channels to be latched. Reading a particular channel will disengage the latch for that channel. Writing a 0 to this register will disengage latch on all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
LATCH	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Test Angle

Type: 16-bit unsigned integer
Range: 0 to 359.9945 degrees
Read/Write: W
Initialized Value: 30°

Enter the D0 test angle as per table.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	approximate value
TEST ANGLE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Degrees)

Two Speed Lock-Loss

Type: binary word
Range: N/A
Read/Write: R
Initialized Value: N/A

When two Synchros are geared to each other, either electrically or mechanically, in order to achieve higher accuracy the misalignment of the Coarse and Fine Synchros must not exceed 90°/gear ratio or the digital angle output may not be valid. Should this problem occur within a given channel pair, the corresponding bit in the *Two-Speed Lock-Loss* register will be set to "0".

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
LATCH	X	X	X	X	X	X	X	X	X	X	X	X	X	¾	X	½	CHANNEL PAIR

Velocity Scale

Type: 16 bit unsigned integer
Range: 9.5367 RPS to 152.5878 RPS
Read/Write: R/W
Initialized Value: N/A

The velocity scale factor is used to achieve a greater resolution at lower rotational speeds (RPS). The scale factor is: **4095(152.5878RPS/max RPS),** where the max RPS is selected by the user to achieve the maximum resolution for a desired RPS. Enter the scale factor as an integer to the corresponding *Velocity Scale* register for that particular channel.

To scale the Max Velocity word for 152.5878 RPS, set Velocity Scale Factor = 4095 (max velocity word of +32,767 (7FFFh) being 152.5878 RPS for CW rotation, and -32,768 (8000h) being 152.5878 RPS for CCW rotation). Scaling effects only the Velocity output word and not the dynamic performance.

To get a maximum velocity word (32,767) @ 152.5878 RPS, Scale Factor = 4095(152.5878/152.5878) = 4095 = 0FFFh;
This results in a velocity resolution of: (152.5878 RPS/32,767) x 360°/RPS = 1.676°/sec (factory default)

To get a maximum velocity word (32,767) @ 50.8626 RPS, Scale Factor = 4095(152.5878/50.8626) = 12,285 = 2FFDh);
This is a velocity resolution of: (50.8626 RPS/32,767) x 360°/RPS = 0.5588°/sec

For 9.5367 RPS max, Scale Factor = 4095(152.5878/9.5367) = 65,520 = FFF0h; 0.10477 °/sec res. (lowest setting)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
VELOCITY SCALE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

A & B Resolution

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Individually configure encoder output resolution or commutation for each channel.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
A & B RESOLUTION	D	X	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D=DATABIT
Integer 0	0													0	0	0	16 bit Encoder Resolution
Integer 1	0													0	0	1	15 bit Encoder Resolution
Integer 2	0													0	1	0	14 bit Encoder Resolution
Integer 3	0													0	1	1	13 bit Encoder Resolution
Integer 4	0													1	0	0	12 bit Encoder Resolution
Integer 32768	1													0	0	0	4 Pole Commutation
Integer 32769	1													0	0	1	6 Pole Commutation
Integer 32770	1													0	1	0	8 Pole Commutation

Bandwidth

Type: Unsigned Integer
Range: N/A
Read/Write: R/W
Initialized Value: N/A

The bandwidth for each channel is individually programmable. The minimum BW is 2 Hz, and the maximum BW is 1000Hz. LSB is 1 Hz. Write desired BW as unsigned integer, between 2 and 1000, to associated channel register. All values greater than 1000 will be processed as 1000Hz. All values less than 2 will be processed as 2Hz. Ex: BW of 40 Hz = 028h

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Bandwidth	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Synchro / Resolver

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Individually configure each channel for Synchro=1 or Resolver=0 measurement.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SYNCHRO / RESOLVER	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	CHANNEL BIT

Reference Frequency

Type: 16-bit unsigned integer
Range: 360 to 10,000 Hz
Read/Write: R/W
Initialized Value: N/A (S/R or L/R module Dependant)

Program Reference Frequency, where LSB is 1 Hz. For Example, 400 Hz = 0000 0001 1001 0000. Reference Module is Optional.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	-	8192	4096	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	approximate value
FREQUENCY	**X**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT (Hz)

Reference Voltage

Type: 16-bit unsigned integer
Range: 2.0 to 28.0 Vrms
Read/Write: R/W
Initialized Value: N/A (S/R or L/R module Dependant)

Program Reference Voltage, where LSB is 0.1 Vrms. For Example, 26.1 Vrms = 0000 0001 0000 0101. Reference Module is Optional.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	-	-	-	-	-	-	-	25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	approximate value
VOLTAGE	**X**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT (Vrms)

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII “1” in upper byte and ASCII space in lower byte for Module Design Version “1 ” is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII “1”								**ASCII “ ”**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII “B” in upper byte and ASCII space in lower byte for Module Design Revision “B ” is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII “B”								**ASCII “ ”**								

Module DSP

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 5331h

Read register to determine Module ID in ASCII. For example, find ASCII “S” in upper byte and ASCII “1” in lower byte, for Module “S1,” together 5331h. Slot 4 will be populated with an “S1” module for 4 or 8 channel applications. Slot 5 will be populated with an “S1” only in 8 channel applications. Slot 6 will be unused “Z0”.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “S”								ASCII “1”								

BIT Status

Type: binary word
Range: 0 to 15
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel’s Built-In-Test (BIT) Status. Channel Status Data bit (Chn, where n is 1, 2, 3 or 4) is fail, high true, and indicates that the channel is not operating spec compliant. Status is latched. Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Signal Status
Type: binary word
Range: N/A
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Signal Status. Status data bit is fail high true and indicates each a Signal input loss to that channel. Signal Loss is indicated after 2 seconds. Signal input monitoring is disabled during D3 or D0 Test. Any Signal Status failure, transient or intermittent will latch the *Signal Status* register. Reading any status bit will unlatch the entire register. Signal Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Open Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Reference Status
Type: binary word
Range: N/A
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Reference Status. Status data bit is fail high true and indicates each a Reference input loss to that channel. Signal and/or Reference Loss is indicated after 2 seconds. Signal and Reference input monitoring is disabled during D3 or D0 Test. Any Reference Status failure, transient or intermittent will latch the *Reference Status* register. Reading any status bit will unlatch the entire register. Reference Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Over-Current Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
REFERENCE STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Angle Δ Alert
Type: binary word
Range: 0 to 15
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Angle Δ Alert Status. Angle Δ Alert Status Data bit (Chn, where n is 1 to 8) is fail, high true, and indicates that the angle position of that channel has exceeded the minimum differential angle specified in the *Angle Δ* register. Status is latched. Reading any status bit will unlatch the entire register. Angle Change Alert part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Max-Hi Threshold Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE Δ ALERT	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

BIT Status Interrupt Enable
Range: 0 to 15
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 0 to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS INTR ENA	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

Signal Status Interrupt Enable

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal (open) status (signal or reference input loss) will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Open Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS INTERRUPT ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	INTERRUPT ENABLE

Reference Status Interrupt Enable

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal (open) status (signal or reference input loss) will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Over-Current Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
REFERENCE STATUS INTERRUPT ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	INTERRUPT ENABLE

Angle Δ Alert Interrupt Enable

Type: binary word
Range: 0 to 15
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, an angle Δ alert will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Max-Hi Threshold Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE Δ INTR ENA	X	X	X	X	X	X	X	X	X	X	X	X	**Ch4**	**Ch3**	**Ch2**	**Ch1**	INTERRUPT ENABLE

L(R)VDT MEASUREMENT (MODULE L*)

PRINCIPAL OF OPERATION (LVDT):

Typically the primary is excited by an ac source, causing a magnetic flux to be generated within the transducer. Voltages are induced in the two secondaries, with the magnitude varying with the position of the core. Usually, the secondaries are connected in series opposition, causing a net output voltage of zero when the core is at the electrical center. When the core is displaced in either direction from center the voltage increases linearly either in phase or out of phase with the excitation depending on the direction.

Interfacing LVDT to Converter

Two common connection methods are:

1. Primary as reference (Two-wire system)
2. Derived reference (Three/four-wire LVDT)

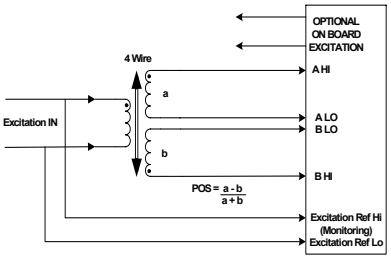
Two-wire system:

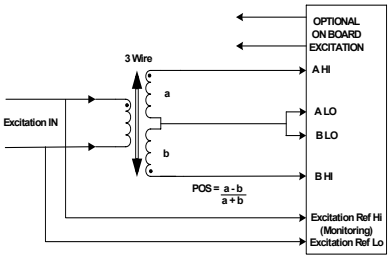
This method of connection converts the widest range of LVDT sensors and. is the most sensitive to excitation voltage variations, temperature and phase shift effects.

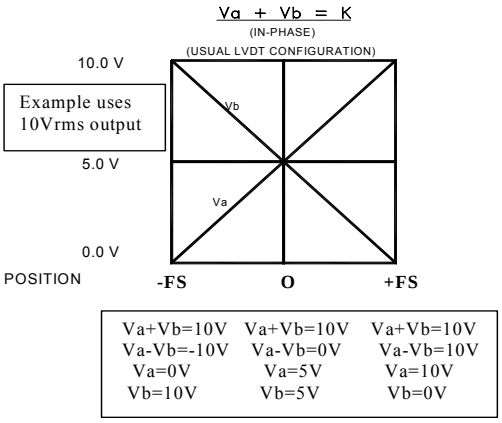
Three / Four -wire system:

The LVDT is again excited from the primary side, but the converter reference is the sum of A + B that has constant amplitude for changing core displacement This system is insensitive to temperature effects, phase shifts and oscillator instability and solves the identity (A-B)/(A+B)

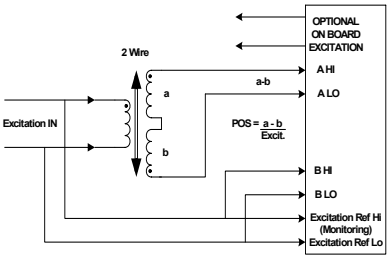
Various LVDT configurations







Va+Vb=10V	Va+Vb=10V	Va+Vb=10V
Va-Vb=-10V	Va-Vb=0V	Va-Vb=10V
Va=0V	Va=5V	Va=10V
Vb=10V	Vb=5V	Vb=0V



Two-LVDT Connections:

Connect A–B LVDT output to Signal A and the Excitation to Signal B inputs. Excitation should also be connected to the Excitation input to enable card to sense and report any excitation loss.

Three or Four-wire LVDT Connections:

Connect A and B LVDT outputs to Signal A and B inputs. Excitation is not used, but should be connected to enable card to sense and report any excitation loss.

L(R)/D MEMORY MAP

000	Position CH 1 Data Lo	R				100	CH1 Signal Loss Threshold	W/R
004	Position CH 1 Data Hi	R				104	CH2 Signal Loss Threshold	W/R
008	Position CH 2 Data Lo	R				108	CH3 Signal Loss Threshold	W/R
00C	Position CH 2 Data Hi	R				10C	CH4 Signal Loss Threshold	W/R
010	Position CH 3 Data Lo	R				110	CH1 REF Loss Threshold	W/R
014	Position CH 3 Data Hi	R				114	CH2 REF Loss Threshold	W/R
018	Position CH 4 Data Lo	R	0A0	CH1 Frequency LO	R	118	CH3 REF Loss Threshold	W/R
01C	Position CH 4 Data Hi	R	0A4	CH1 Frequency HI	R	11C	CH4 REF Loss Threshold	W/R
020	CH1 VEL Lo	R	0A8	CH2 Frequency LO	R	120	CH1 VEL SCALE	W/R
024	CH 1 VEL HI	R	0AC	CH2 Frequency HI	R	124	CH2 VEL SCALE	W/R
028	CH 2 VEL Lo	R	0B0	CH3 Frequency LO	R	128	CH3 VEL SCALE	W/R
02C	CH 2 VEL HI	R	0B4	CH3 Frequency HI	R	12C	CH4 VEL SCALE	W/R
030	CH 3 VEL Lo	R	0B8	CH4 Frequency LO	R	13C	SIG Status Ch.1-4	R
034	CH 3 VEL HI	R	0BC	CH4 Frequency HI	R	140	REF Status Ch.1-4	R
038	CH 4 VEL Lo	R	0C0	CH1 VLL (A+B Magnitude)	R	144	BIT Status Ch.1-4	R
03C	CH 4 VEL HI	R	0C4	CH2 VLL (A+B Magnitude)	R	148	LD Lock Status Ch.1-4	R
040	CH 1 Bandwidth	R/W	0C8	CH3 VLL (A+B Magnitude)	R			
044	CH 2 Bandwidth	R/W	0CC	CH4 VLL (A+B Magnitude)	R	150	SIG Status Interrupt Enable Ch.1-4	R/W
048	CH 3 Bandwidth	R/W	0D0	CH1 REF	R	154	REF Status Interrupt Enable Ch.1-4	R/W
04C	CH 4 Bandwidth	R/W	0D4	CH2 REF	R	158	BIT Status Interrupt Enable Ch.1-4	R/W
050	Bandwidth Select	R/W	0D8	CH3 REF	R	15C	LD Lock Status Interrupt Enable Ch.1-4	R/W
			0DC	CH4 REF	R			
						200	OSC Freq Lo	W/R
05C	LD Active Channels	R/W				204	OSC Freq HI	W/R
060	LD Track / Hold	R/W				208	OSC Volt Lo	W/R
064	D2 Test Verify	R/W				20C	OSC Volt Hi	W/R
068	Test Enable	R/W						
06C	Test Angle	R/W						
400	Vector Signal Loss	W/R				768	Module Design Version	
404	Vector REF Loss	W/R				770	Module DSP Rev	W/R
408	Vector BIT Fail	W/R				774	Module FPGA Rev	W/R
40C	Vector Lock Loss	W/R				778	Module ID	R
410	Vector Angle Δ	W/R				76C	Module Design Revision	

(LVDT data buffering pending)

Programming Descriptions

At Power ON or system reset, all parameters are restored to default setup.

Enter Active channels: Set the bit, corresponding to each channel to be monitored during BIT testing, in the Active Channel register ("1"=active; "0"=not used). Omitting this step will produce false alarms because unused channels will set faults.

Read Position Data: Read the Position Data Register corresponding to a given channel.

Data Format (2-wire): The output data is A / B and represents %FS. Format is two's complement. Max. positive excursion is 7FFF, 0 = 0, and max. negative excursion is 8000.

Data Format (4-wire): The output data is A-B/A+B and represents %FS. Format is two's complement. Max. positive excursion is 7FFF, 0 = 0, and max. negative excursion is 8000.

Latch the position data for all channels by writing "1" to D1 of Latch register. Reading channel will disengage latch for that channel.

Programming Signal Scale:

For two wire applications the **Signal Scale** registers should be set to the Transformation Ratio of the LVDT, so that full scale output code is reached at full travel.

For 3 or 4 wire applications the LVDT has two output voltages referred to as A and B. When connected to the A and B Signal inputs no scaling is required because the inputs are Autoranging, however the signal register can be used to scale the output code.

The default setting for the **Signal Scale** registers are FFFFh. This results in a full scale output reading for full travel of the LVDT. A full scale output reading for less then full travel of the LVDT can be programmed by writing to the Signal registers. For example writing 8000h to the **Signal Scale** Register for channel 1 will result in channel 1 having a full scale output reading for one half travel of the LVDT

(A+B) output magnitude: Read 16 bit word, at appropriate register, and multiply by 0.01 Volt to read the magnitude, of the sum, of signals A & B.

Velocity Scale Factor:

To scale the Max Velocity word for 150 Strokes / Second (SpS), set Velocity Scale Factor = 4095 in HEX (max velocity word of 7FFFh being max. CW rotation, and 8000h being max. CCW rotation).
Scaling effects **only** the Velocity output word and not the dynamic performance.

Ex: To get max. velocity word @ 150 SPS: 4095(150/150) = 4095 (0FFFh) This is also the Factory setting.

To get max. velocity word @ 50 SPS. 4095(150/50) = 12,285 (2FFDh)

To get max. velocity word @ 9.375 SPS.4095(150/9.375) = 65,520 (FFF0h) This is also the lowest setting.

Velocity Output: Read Velocity registers of each channel as a 2's complement word, with 7FFFh being max. CW rotation, and 8000h being max. CCW rotation.

When max. velocity is set to 150 SpS, an actual speed of 10 SpS CW would be read as 0888h.
When max. velocity is set to 150 SpS, an actual speed of 10 SpS CCW would be read as F778h.
When max. velocity is set to 50 SpS, an actual speed of 10 SpS CW would be read as 1999h.
When max. velocity is set to 50 SpS, an actual speed of 10 SpS CCW would be read as E667h.

To convert a velocity word, for example E667h, into rps: If max. velocity set to 50 SpS, then
SpS = 50 x E667h / 32,768 = 50 x -6,553 / 32,768 = -10 SpS

2 Wire / 4 Wire Select: Write a "1" to the bit corresponding to the channel, to be programmed, for two wire operation. Write a "0" for 3 or 4 Wire operation.

Bandwidth
The bandwidth for each channel is individually programmable. The minimum BW is 2 Hz, and the maximum BW is 1000Hz. LSB is 1 Hz. Write desired BW as unsigned integer, between 2 and 1000, to associated channel register. All values greater than 1000 will be processed as 1000Hz. All values less than 2 will be processed as 2Hz.

Input Reference Frequency Measurement
Each individual channel input reference frequency is measured and the value reported to a corresponding read register. The input reference frequency is reported to a resolution of 0.01 Hz. The output is in integer decimal format. For example, if channel 1 input reference is 400 Hz, the output measurement word from the corresponding register would be 40000.

Input Signal Voltage (VLL) Measurement
Each individual channel input signal voltage "VLL" is measured and the value reported to a corresponding read register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input signal voltage is 11.8 Vrms, the output measurement word from the corresponding register would be 1180.

Input Reference Loss Detection Threshold
Each individual channel input reference voltage is measured. By setting the Input Reference Loss detection threshold, the user has capability of tailoring when reference loss detection is indicated during the D2 background test. The reference loss threshold is set by entering the voltage level in decimal integer format to a resolution of 10 mv. For example, if the user wishes channel 1 reference loss threshold set for 2 Vrms, the register would be set to 200.

Input Signal Loss Detection Threshold
Each individual channel input signal voltage is measured. By setting the Input Signal Loss detection threshold, the user has capability of tailoring when signal loss detection is indicated during the D2 background test. The signal loss threshold is set by entering the voltage level in decimal integer format to a resolution of 10 mv. For example, if the user wishes channel 1 signal loss threshold set for 4 Vrms, the register would be set to 400.

Test Enable (D3): Writing "1" to D3 of Test Enable register initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates multiple positive test voltages that are measured to a test accuracy of 0.1%FS. Test cycle takes about 45 seconds and results can be read from the status registers when D3 changes from "1" to "0". External excitation is not required. Testing requires no external programming and can be initiated or terminated (by setting D3 to "0") via the bus.

Test Enable (D2): Writing “1” to D2 of Test Enable register, initiates automatic background BIT testing. Each channel is checked over the programmed Signal range to a measuring accuracy 0.1%FS, and each Signal and Excitation is monitored. The results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. The card will write 55h to the test D2 verify register when D2 is enabled. User can periodically clear to 0 and then read the test D2 verify register again, after 30 seconds, to verify that background BIT testing is activated.

Test Enable (D0): Checks the card and the PCbus interface. Writing “1” to D0 of Test Enable register disconnects all channels from the outside world, allowing user to write any number of input positions to the card at Test Enable register and then read the data from the PCbus interface (allow 400 ms after writing). External excitation is not required.

Status, Sig: Check the corresponding bit of the Sig Status register for status of the input signals for each active channel. A "1" = Signal ON, “0” = Signal loss. (Signal loss is detected after 2 seconds)

Status, Exc: Check the corresponding bit of the Exc Status register for status of the excitation input for each active channel. A ”1” =Exc. ON, “0” = Exc. Loss. (Excitation loss is detected after 2 seconds)

Status, Test: Check the corresponding bit of the Test Status register for status of D2 or D3 BIT testing for each active channel. A ”1” Accuracy OK; “0” failed. (D3 test cycle takes 45 seconds for accuracy error).

(A&B) Encoder Resolution: Enter required resolution, for each channel, per above table. Can be changed on the fly. Encoder outputs are optional, see part ordering information. Default is 12 bit encoder output.

Bank Select for Digital I/O's: Controls the direction of each bank of 8, Digital I/O. A "0" in a bank register set the corresponding bank to be an Inputs. A "1" sets the bank to be Outputs.

Input Register: Indicates the logic state of Digital I/O bits. Upper byte represents bank 8 – 15, lower byte represents bank 0 – 7.

Output Register: Controls the logic state of Digital I/O bits, when bank is set to be Outputs. Upper byte controls bank 8 – 15, lower byte controls bank 0 – 7.

Soft reset: (Level sensitive): “1” to Soft Reset register initiates and holds software in reset state. Then, writing “0” initiates reboot (takes 400 ms). This function is equivalent to a power-on reset.

GENERAL USE REGISTER MEMORY MAP

The registers of this memory map apply to the complete card. The *Test Enable* and related registers affect all modules unless otherwise specified. BIT tests are module dependant. See module description for details.

GENERAL USE MEMORY MAP

3000	Part number	R	3024	Latch All A/Ds[1]	R/W	3400	Interrupt Status	R/W
3004	Serial number	R				3404	Interrupt Status Clear	R/W
3008	Date Code	R				3408	Interrupt Vector	R/W
300C	Rev. Level, PCB	R				340C	Soft Reset	W
3010	Rev. Level, Processor 1	R						
3014	Rev. Level, PCI FPGA	R						
			3030	Design Version	R			
			3034	Platform	R			
3018	Board Ready	R	3038	Model	R			
301C	Watchdog Timer	R/W	303C	Generation	R			
3020	Soft reset	W	3040	Special Spec	R			

Address to General Use Registers has NO MODULE OFFSET.

Note: 1. Only affects A/D Modules.

Part Number

is read as a 16 bit binary word. A unique 16 bit code is assigned to each model number.

Serial Number

is read as a 16 bit binary word.

Date Code

Read as a decimal number. The four digits represent YYWW (Year, Year, Week, Week)

Revisions

Read as a 16 bit binary word

Board Ready

Poll register. Board is ready to be accessed **only after** you read “AA55”. (within 1 second after board power-on)

Watchdog timer

This feature monitors the watchdog timer register. When it detects that a code has been received, that code will be inverted within 100 µSec. The inverted code stays in the register until replaced by a new code. After 100 µSec. elapse, look for the inverted code to confirm that the processor is operating.

Soft reset

Soft Reset is Level sensitive. Writing a “1” initiates and holds software in reset state; then writing “0” initiates reboot (depending upon configuration, takes up to 3 seconds). This function is equivalent to a power-on reset where all parameters are reset to their default condition.

Test Enable

Set bit to enable associated Built-In Self Test D3, D2, or D0. Each test affects each Module Type differently. See the individual module section for test description(s).

Write "1" to D2 to initiate automatic background BIT testing. Card will (every 30 seconds) write 55h at *Test (D2) verification* register when D2 is enabled. User can periodically clear to 00h and then read *Test (D2) verification* register again, after 30 seconds, to verify that background bit testing is activated. D3 test cycle is completed within 45 seconds and results can be read from the associated status registers when D3 changes from "1" to "0". Any failure triggers an Interrupt (if enabled). All testing requires no external programming and is initiated by writing "1" or terminated by writing "0".

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0

Test (D2) Verify

Card will (every 30 seconds) write 55h at *Test (D2) Verification* register when (D2) is enabled. User can periodically clear to 00h and then read again, after 30 seconds, to verify that background bit testing is activated.

Latch All A/Ds

Latch all A/D channels by writing "1" to D1 of Latch register. Write "0" to unlatch all channels.

A/D D0 Test Range

Specify voltage range for A/D module under test. D0 test is performed only on A/D modules. Enter per table:

A/D	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D0 Test Range	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D	D

Range					
40.0 V	*	1	0	1	0
20.0 V	*	1	0	0	1
10.0 V	*	0	0	0	0
5.00 V	*	0	0	0	1
2.50 V	*	0	0	1	0
1.25 V	*	0	0	1	1
0.625 V	*	0	1	0	0

∗ For bipolar/unipolar selection, program D4 as "0" for unipolar and "1" for bipolar.

A/D D0 Test Voltage

Specify voltage to be applied by D0 test to A/D module under test. D0 test is performed only on A/D modules. If using bi-polar mode, write 16 bit 2's complement word (7FFFh=+FS, 8000h=-FS). If using uni-polar mode, write 16 bit binary word (range: 0 to FFFFh=FS).

Example 1: if using uni-polar mode with 10v range, enter 8000h for 5v test voltage.
Example 2: if using bi-polar mode with 10v range, enter 4000h for 5v test voltage. Enter C000h for –5v.

D/A Reset to Zero

Write "1" to drive all D/A outputs to zero. When complete, *D/A Reset to Zero* register will be automatically set to "0".

D/A Retry Overload

Write "1" to *D/A Retry overload* register to enable all channels (board wide) whose outputs were previously set to zero because of an overload condition. If and overload condition still exists, the channel output(s) will again be set to zero. While enabled, all overloaded channel outputs will be again be reset approximately every second. Default is "0".

D/A Reset Overload

This register is used to reset all channels whose outputs were previously set to zero because of an overload. If an overload condition still exists, channel output(s) will again be set to zero. Channel output reset will occur one time only. *D/A Reset overload* register is be automatically reset to 0 after channel output reset activity is complete. Card will attempt to reset channel output(s) once for every time "1" is written to the register.

D/A Override

Write “1” at *Override* register to turn ON all overloaded outputs, short life condition.

Design Version

The register holds product design version in ASCII. For example, design version 1 would be ASCII “1” is in upper byte and ASCII “space” in lower byte, together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODEL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “1 ”								ASCII “ ”								

Platform

This register holds PCI platform code “76” in ASCII. Find ASCII “7” is in upper byte and ASCII “6” in lower byte, together 3736h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PLATFORM	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “7”								ASCII “8”								

Model

The register holds product model code “C ” in ASCII. Find ASCII “C” is in upper byte and ASCII “space”in lower byte, together 4320h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODEL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “C”								ASCII “”								

Generation

This register holds product generation code “1 ” in ASCII. Find ASCII “1” is in upper byte and ASCII “space” in lower byte, together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
GENERATION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “1”								ASCII “”								

Special Spec

This register holds product special specification code in ASCII. Find ASCII space used for none where ASCII “space” is in upper and lower bytes, together 2020h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt Status

Poll this register to determine interrupt status. Logic “1” indicates interrupt service is required; logic “0” indicates no interrupt requires servicing.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Interrupt Clear

Use this register to clear interrupt; usually cleared by user interrupt service routine. Enter logic “1” to indicate interrupt service complete. Register is cleared to logic “0” by the processor to acknowledge interrupt removal.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

REFERENCE (W1)

(PENDING – CONTACT FACTORY FOR DETAILS)

For frequency, write a 16-bit integer to the *Frequency Ref Supply Register*. (Ex: 400 Hz = 0190h) with LSB= 1Hz.

For voltage, write a 16-bit integer to the *Voltage Ref Supply Register*. (Ex: 26Vrms =0104h) with LSB=0.1Vrms.

It is recommended that the user program the required frequency before setting the output voltage.

EXTERNAL +/- 12VDC POWER: (JP10 & JP11)

The card is shipped and configured for operation with +/- 12 VDC power, being supplied from the PCI Bus edge connector (PCI Bus Power).

To operate from External +/- 12VDC supplies: On jumper block JP11, remove jumpers 1-2, and 5-6, then re-connect jumpers 3-4 and 7-8. Leave jumper 9 – 10 connected (PCI Bus GND).

Connect external +12 VDC to JP10-4; connect external -12 VDC to JP10-2 and external ground to JP10-1.

FRONT AND CARD CONNECTORS

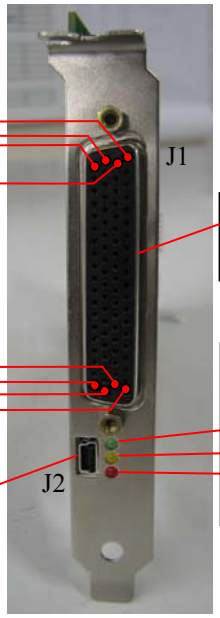
Connector Summary:

Designator	Description / Use	Type
J1	Front Panel Main I/O	AMP 748483-5 Mate: AMP 748368-1 (or equivalent)
J2	Factory Use Only (utilized for FW download)	Mini-B J style
JP1	Factory Use Only	N/A
JP4	Factory Use Only	N/A
JP9	Optional Encoder/Commutation I/O	Samtec TSW-125-25-T-D-RA
JP10	External +/- 12 VDC INPUT connector Used in conjunction with JP11 – when utilized, user may provide an external +/- 12 VDC power source	Samtec TSW-104-14-L-S
JP11	Shunt Selector Header for +/- 12 VDC source (May be used in conjunction with JP10) Shunt JP11-1,2 and 5,6 for PCI +/-12 VDC (respectively) Or Shunt JP11-3,4 and 7,8 for External (via JP10) +/- 12VDC respectively	Samtec TSW-105-14-L-D

See Pinouts / Designations on following pages

DO NOT CONNECT TO ANY UNDESIGNATED, (NC) or "Factory Use" PINS

CONNECTOR / LED PLACEMENT / DESIGNATIONS



J1 Front Panel Connector
AMP 748483-5

Front Panel LEDs [normal operation]

	** Illuminated**	** Extinguished **
GRN	[Module(s) config OK]	Module(s) config Fail
YEL	[Card Access]	[No Card Access]
RED	Built-In-Test (BIT) Failed	[BIT OK]

J2 Industry Standard USB-(Mini-B J style)
(for factory use only)

Front Panel Connector / LED Designations

JP11 – Jumper Header for choosing External or PCI Bus +/- 12 VDC INPUT
(Samtec TSW-105-14-L-D)

Shunt JP11-1, 2 and JP11- 5, 6 for PCI +/-12 VDC (respectively) (factory default)
Or
Shunt JP11 - 3, 4 and JP11 - 7, 8 for External (via JP10) +/- 12VDC respectively

(Used in conjunction w/ JP10)

JP10 – External +/- 12 VDC INPUT
(Samtec TSW-104-14-L-S)

(Used in conjunction w/ JP11)

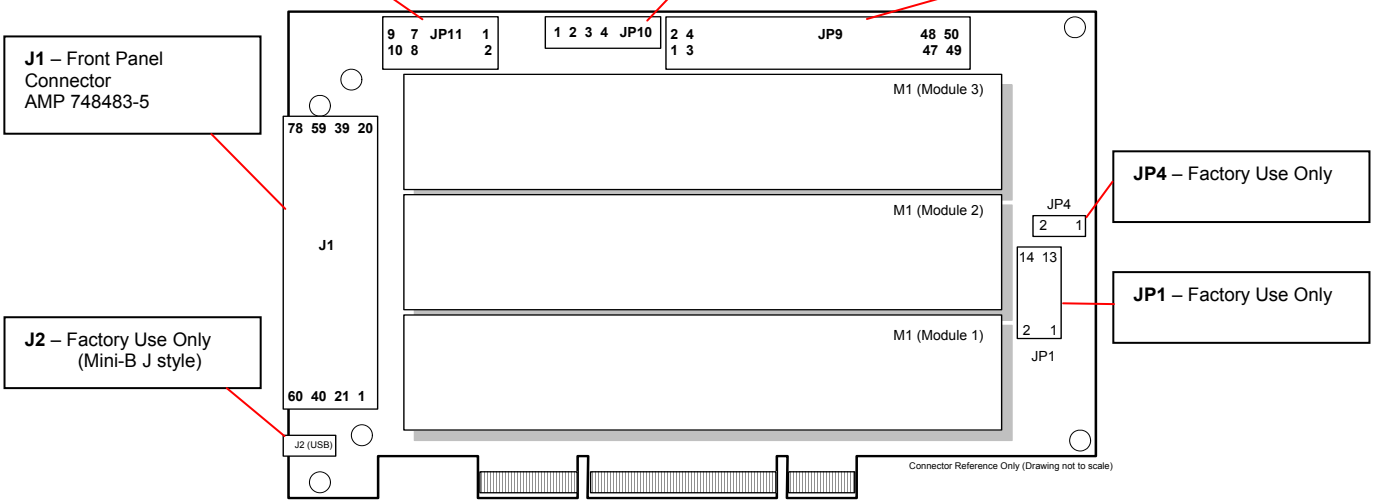
JP9 – Optional Encoder/Commutation
(Samtec TSW-125-25-T-D-RA)

J1 – Front Panel Connector
AMP 748483-5

J2 – Factory Use Only
(Mini-B J style)

JP4 – Factory Use Only

JP1 – Factory Use Only



Board Connector Designations

SLOT 1 – Connector Pin-Out

SLOT 1	78-pin	S/D	Note 4 I/O (K6)	Note 6 TTL (D7)	DIFF (D8)	REF (W1)	AD	Note 7 DA	Note 7 DA (J7)	Note 7 DA-HI-CURR	RTD (G4)	Note 8 FREQ (E5)
	J1-1	S1-CH1	IO-CH1	IO-CH1	IOHI-CH1		IN1+	CH1-H	CH1-H	CH1-H	DRV+N1	
	J1-21	S3-CH1	IO-CH2	IO-CH2	IOLO-CH1		IN1-	CH1-L	CH1-L	CH1-L	DRV-N1	
	J1-2	S2-CH1	IO-CH3	IO-CH3	IOHI-CH2		IN2+	CH2-H		CH1-SNSH	SNS+N1	
	J1-22	S4-CH1	IO-CH4	IO-CH4	IOLO-CH2		IN2-	CH2-L		CH1-SNSL	SNS-N1	
	J1-3	RHI-CH1	VCC1	VCC1	IOHI-CH3	RHI-OUT	IN3+	CH3-H			DRV+N2	
	J1-23	RLO-CH1	GND1	GND1	IOLO-CH3	RLO-OUT	IN3-	CH3-L			DRV-N2	
	J1-4	S1-CH2	IO-CH5	IO-CH5	IOHI-CH4		IN4+	CH4-H	CH2-H	CH2-H	SNS+N2	CH1
	J1-24	S3-CH2	IO-CH6	IO-CH6	IOLO-CH4		IN4-	CH4-L	CH2-L	CH2-L	SNS-N2	GND
	J1-5	S2-CH2	IO-CH7	IO-CH7	IOHI-CH5		IN5+	CH5-H		CH2-SNSH	DRV+N3	
	J1-25	S4-CH2	IO-CH8	IO-CH8	IOLO-CH5		IN5-	CH5-L		CH2-SNSL	DRV-N3	
	J1-6	RHI-CH2	VCC2	VCC2	IOHI-CH6		GND		+VIN 1-2		SNS+N3	CH2
	J1-26	RLO-CH2	GND2	GND2	IOLO-CH6				-VIN 1-2		SNS-N3	GND
	J1-40	S1-CH3	IO-CH9	IO-CH9	GND		IN6+	CH6-H	CH3-H	CH3-H	DRV+N4	
	J1-60	S3-CH3	IO-CH10	IO-CH10	GND		IN6-	CH6-L	CH3-L	CH3-L	DRV-N4	
	J1-41	S2-CH3	IO-CH11	IO-CH11	IOHI-CH7		IN7+	CH7-H		CH3-SNSH	SNS+N4	CH3
	J1-61	S4-CH3	IO-CH12	IO-CH12	IOLO-CH7		IN7-	CH7-L		CH3-SNSL	SNS-N4	GND
	J1-42	RHI-CH3	VCC3	VCC3	IOHI-CH8		IN8+	CH8-H			DRV+N5	
	J1-62	RLO-CH3	GND3	GND3	IOLO-CH8		IN8-	CH8-L			DRV-N5	
	J1-43	S1-CH4	IO-CH13	IO-CH13	IOHI-CH9		IN9+	CH9-H	CH4-H	CH4-H	SNS+N5	CH4
	J1-63	S3-CH4	IO-CH14	IO-CH14	IOLO-CH9		IN9-	CH9-L	CH4-L	CH4-L	SNS-N5	
	J1-44	S2-CH4	IO-CH15	IO-CH15	IOHI-CH10		IN10+	CH10-H		CH4-SNSH	DRV+N6	GND
	J1-64	S4-CH4	IO-CH16	IO-CH16	IOLO-CH10		IN10-	CH10-L		CH4-SNSL	DRV-N6	
	J1-45	RHI-CH4	VCC4	VCC4	IOHI-CH11				+VIN 3-4		SNS+N6	
	J1-65	RLO-CH4	GND4	GND4	IOLO-CH11				-VIN 3-4		SNS-N6	

SLOT 2 – Connector Pin-Out

SLOT 2	78-Pin	S/D	Note 4 I/O (K6)	Note 6 TTL (D7)	DIFF (D8)	REF (W1)	AD	Note 7 DA	Note 7 DA (J8)	Note 7 DA-HI-CURR	RTD G4)	Note 8 FREQ (E5)
	J1-27	S1-CH1	IO-CH1	IO-CH1	IOHI-CH1		IN1+	CH1-H	CH1-H	CH1-H	DRV+N1	
	J1-8	S3-CH1	IO-CH2	IO-CH2	IOLO-CH1		IN1-	CH1-L	CH1-L	CH1-L	DRV-N1	
	J1-28	S2-CH1	IO-CH3	IO-CH3	IOHI-CH2		IN2+	CH2-H		CH1-SNSH	SNS+N1	
	J1-9	S4-CH1	IO-CH4	IO-CH4	IOLO-CH2		IN2-	CH2-L		CH1-SNSL	SNS-N1	
	J1-29	RHI-CH1	VCC1	VCC1	IOHI-CH3	RHI-OUT	IN3+	CH3-H			DRV+N2	
	J1-10	RLO-CH1	GND1	GND1	IOLO-CH3	RLO-OUT	IN3-	CH3-L			DRV-N2	
	J1-30	S1-CH2	IO-CH5	IO-CH5	IOHI-CH4		IN4+	CH4-H	CH2-H	CH2-H	SNS+N2	CH1
	J1-11	S3-CH2	IO-CH6	IO-CH6	IOLO-CH4		IN4-	CH4-L	CH2-L	CH2-L	SNS-N2	GND
	J1-31	S2-CH2	IO-CH7	IO-CH7	IOHI-CH5		IN5+	CH5-H		CH2-SNSH	DRV+N3	
	J1-12	S4-CH2	IO-CH8	IO-CH8	IOLO-CH5		IN5-	CH5-L		CH2-SNSL	DRV-N3	
	J1-32	RHI-CH2	VCC2	VCC2	IOHI-CH6		GND		+VIN 1-2		SNS+N3	CH2
	J1-13	RLO-CH2	GND2	GND2	IOLO-CH6				-VIN 1-2		SNS-N3	GND
	J1-66	S1-CH3	IO-CH9	IO-CH9	GND		IN6+	CH6-H	CH3-H	CH3-H	DRV+N4	
	J1-47	S3-CH3	IO-CH10	IO-CH10	GND		IN6-	CH6-L	CH3-L	CH3-L	DRV-N4	
	J1-67	S2-CH3	IO-CH11	IO-CH11	IOHI-CH7		IN7+	CH7-H		CH3-SNSH	SNS+N4	CH3
	J1-48	S4-CH3	IO-CH12	IO-CH12	IOLO-CH7		IN7-	CH7-L		CH3-SNSL	SNS-N4	GND
	J1-68	RHI-CH3	VCC3	VCC3	IOHI-CH8		IN8+	CH8-H			DRV+N5	
	J1-49	RLO-CH3	GND3	GND3	IOLO-CH8		IN8-	CH8-L			DRV-N5	
	J1-69	S1-CH4	IO-CH13	IO-CH13	IOHI-CH9		IN9+	CH9-H	CH4-H	CH4-H	SNS+N5	CH4
	J1-50	S3-CH4	IO-CH14	IO-CH14	IOLO-CH9		IN9-	CH9-L	CH4-L	CH4-L	SNS-N5	
	J1-70	S2-CH4	IO-CH15	IO-CH15	IOHI-CH10		IN10+	CH10-H		CH4-SNSH	DRV+N6	GND
	J1-51	S4-CH4	IO-CH16	IO-CH16	IOLO-CH10		IN10-	CH10-L		CH4-SNSL	DRV-N6	
	J1-71	RHI-CH4	VCC4	VCC4	IOHI-CH11				+VIN 3-4		SNS+N6	
	J1-52	RLO-CH4	GND4	GND4	IOLO-CH11				-VIN 3-4		SNS-N6	

SLOT 3 – Connector Pin-Out

SLOT 3	78-Pin	S/D	Note 4 I/O (K6)	Note 6 TTL (D7)	DIFF (D8)	REF (W1)	AD	Note 7 DA	Note 7 DA (J8)	Note 7 DA-HI-CURR	RTD G4)	Note 8 FREQ (E5)
	J1-14	S1-CH1	IO-CH1	IO-CH1	IOHI-CH1		IN1+	CH1-H	CH1-H	CH1-H	DRV+N1	
	J1-34	S3-CH1	IO-CH2	IO-CH2	IOLO-CH1		IN1-	CH1-L	CH1-L	CH1-L	DRV-N1	
	J1-15	S2-CH1	IO-CH3	IO-CH3	IOHI-CH2		IN2+	CH2-H		CH1-SNSH	SNS+N1	
	J1-35	S4-CH1	IO-CH4	IO-CH4	IOLO-CH2		IN2-	CH2-L		CH1-SNSL	SNS-N1	
	J1-16	RHI-CH1	VCC1	VCC1	IOHI-CH3	RHI-OUT	IN3+	CH3-H			DRV+N2	
	J1-36	RLO-CH1	GND1	GND1	IOLO-CH3	RLO-OUT	IN3-	CH3-L			DRV-N2	
	J1-17	S1-CH2	IO-CH5	IO-CH5	IOHI-CH4		IN4+	CH4-H	CH2-H	CH2-H	SNS+N2	CH1
	J1-37	S3-CH2	IO-CH6	IO-CH6	IOLO-CH4		IN4-	CH4-L	CH2-L	CH2-L	SNS-N2	GND
	J1-18	S2-CH2	IO-CH7	IO-CH7	IOHI-CH5		IN5+	CH5-H		CH2-SNSH	DRV+N3	
	J1-38	S4-CH2	IO-CH8	IO-CH8	IOLO-CH5		IN5-	CH5-L		CH2-SNSL	DRV-N3	
	J1-19	RHI-CH2	VCC2	VCC2	IOHI-CH6		GND		+VIN 1-2		SNS+N3	CH2
	J1-39	RLO-CH2	GND2	GND2	IOLO-CH6				-VIN 1-2		SNS-N3	GND
	J1-53	S1-CH3	IO-CH9	IO-CH9	GND		IN6+	CH6-H	CH3-H	CH3-H	DRV+N4	
	J1-73	S3-CH3	IO-CH10	IO-CH10	GND		IN6-	CH6-L	CH3-L	CH3-L	DRV-N4	
	J1-54	S2-CH3	IO-CH11	IO-CH11	IOHI-CH7		IN7+	CH7-H		CH3-SNSH	SNS+N4	CH3
	J1-74	S4-CH3	IO-CH12	IO-CH12	IOLO-CH7		IN7-	CH7-L		CH3-SNSL	SNS-N4	GND
	J1-55	RHI-CH3	VCC3	VCC3	IOHI-CH8		IN8+	CH8-H			DRV+N5	
	J1-75	RLO-CH3	GND3	GND3	IOLO-CH8		IN8-	CH8-L			DRV-N5	
	J1-56	S1-CH4	IO-CH13	IO-CH13	IOHI-CH9		IN9+	CH9-H	CH4-H	CH4-H	SNS+N5	CH4
	J1-76	S3-CH4	IO-CH14	IO-CH14	IOLO-CH9		IN9-	CH9-L	CH4-L	CH4-L	SNS-N5	
	J1-57	S2-CH4	IO-CH15	IO-CH15	IOHI-CH10		IN10+	CH10-H		CH4-SNSH	DRV+N6	GND
	J1-77	S4-CH4	IO-CH16	IO-CH16	IOLO-CH10		IN10-	CH10-L		CH4-SNSL	DRV-N6	
	J1-58	RHI-CH4	VCC4	VCC4	IOHI-CH11				+VIN 3-4		SNS+N6	
	J1-78	RLO-CH4	GND4	GND4	IOLO-CH11				-VIN 3-4		SNS-N6	

NOTES: [1] N/A
[2] N/A
[3] N/A
[4] I/O Module (K6) **–** VCC input for banks of four channels (i.e. VCC1 indicates VCC input for CH 1-4, VCC2 indicates input for CH 5-8, etc.) All GND pins are common within the module; however, each pin should be individually wired for optimal power current distribution.
[5] N/A
[6] TTL Modules -- Outputs referenced to PCI GND
[7] D/A Module -- ALL D/A Low signals are connected to AGND; Common to the module, isolated from all other modules and PCI GND.
[8] Freq Module -- ALL channels GND is independent per channel / module and isolated from PCI GND

AGND/NC is AGND for A/D Module, and NO CONNECT for D/A Module.

ALL D/A Low signals (MxChxx Sig L) are connected to AGND, Common within that module, isolated from all other modules and isolated from the PCI bus.

For DISCRETE Modules, where n=1 to 3, MnGnd1-4, MnGnd5-8, MnGnd9-12 and McGnd13-16 are all common for that module. However, each pin should be individually wired for optimal power current distribution throughout that module. MnGnd and MnVcc MUST be wired for proper operation.

Encoder/Commutation Outputs

Connector : JP9 Samtec TSW-125-25-T-D-RA

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	A Hi Ch1	15	B Hi Ch3	31	IDX Hi Ch5	45	A Hi Ch8
2	A Lo Ch1	16	B Lo Ch3	32	IDX Lo Ch5	46	A Lo Ch8
3	B Hi Ch1	17	IDX Hi Ch3	33	A Hi Ch6	47	B Hi Ch8
4	B Lo Ch1	18	IDX Lo Ch3	34	A Lo Ch6	48	B Lo Ch8
5	IDX Hi Ch1	19	A Hi Ch4	35	B Hi Ch6	49	IDX Hi Ch8
6	IDX Lo Ch1	20	A Lo Ch4	36	B Lo Ch6	50	IDX Lo Ch8
7	A Hi Ch2	21	B Hi Ch4	37	IDX Hi Ch6		
8	A Lo Ch2	22	B Lo Ch4	38	IDX Lo Ch6	25	GROUND
9	B Hi Ch2	23	IDX Hi Ch4	39	A Hi Ch7	26	GROUND
10	B Lo Ch2	24	IDX Lo Ch4	40	A Lo Ch7		
11	IDX Hi Ch2	27	A Hi Ch5	41	B Hi Ch7		
12	IDX Lo Ch2	28	A Lo Ch5	42	B Lo Ch7		
13	A Hi Ch3	29	B Hi Ch5	43	IDX Hi Ch7		
14	A Lo Ch3	30	B Lo Ch5	44	IDX Lo Ch7		

TABLE 9

Notes:
1. Commutation outputs are differential outputs and are translated as follows:
   A = Ch1 A HI & LO; B = Ch1 B HI & LO; C = Ch1 IDX HI & LO
2. Encoder/Commutation Outputs are available only for Modules 1 and 2 (8 channels max).

PART NUMBER DESIGNATION

76C2 –XX XX XX X X –XX
Slot # 1 2 3

Module (Slot) Definition

Enter Module (code) for each of Slots 1 through 6; "Z0" if slot not used

A/D (C1)	Ten (10) A/D (1.25 VDC to 10.0 VDC FS) Uni or bipolar
A/D (C2)	Ten (10) A/D (40VDC) Uni or bipolar
A/D (C3)	Ten (10) 4 – 20ma Current Measurement Module
A/D (C4)	Ten (10) A/D (50VDC) Uni or bipolar
Signal (E5)	Four (4) Programmable Function Generators
D/A (F1)	Ten (10) D/A Outputs ±10 VDC, PCI ISOLATED
D/A (F3)	Ten (10) D/A Outputs ±5 VDC, PCI ISOLATED
D/A (J3)	Ten (10) D/A Outputs ±1.25 VDC, PCI ISOLATED
D/A (J5)	Ten (10) D/A Outputs ±2.5 VDC, PCI ISOLATED
D/A (J7)	Four (4) D/A Outputs ±20 to ±80 VDC, PCI ISOLATED
I/O TTL (D7)	Sixteen (16) TTL (0-5V), Programmable for Input or Output
I/O Differential (D8)	Eleven (11) Differential Multi-Mode Transceivers
I/O Discrete (K6)	Sixteen (16) Discrete (0-80V), ISOLATED, Programmable for Input or Output
RTD (G4)	Six (6) four-wire Platinum RTD
LVDT (L*) Note 1	Four LVDT or RVDT-to-digital
S/D (S*) Note 2	Four (4) Synchro/Resolver, programmable
Reference (W1)	One 2.2 VA programmable. 2-115 Vrms, 50 Hz-10 KHz

Temperature

C = 0 TO 70 (deg. C)
E = -40 TO +85 (deg, C)
H = E WITH REMOVABLE COATING
K = C WITH REMOVABLE COATING

Encoder / Commutation Outputs (Synchro / Resolver Measurement)

0 = No Encoder / Commutation Outputs
E = Encoder / Commutation Outputs Included (Note 3)

Special Option Code (or leave blank)

(Special Option Code utilized for special R/D specifications or non-standard operation – consult factory)

Part Number Notes:

Note 1: LVDT/RVDT four channel Measurement module selection:

(For ranges other than those listed contact factory. Customer should indicate the actual frequency applicable to his design to assure that the correct default band width is set at the factory.

(Code)	Input voltage	Reference voltage	Frequency band	Remarks
LB	2-28 VL-L	2-28 Vrms	400 Hz-1 KHZ	All Input and Reference voltages are auto ranging
LC	2-28 VL-L	2-28 Vrms	1 KHZ-3 KHZ	All Input and Reference voltages are auto ranging
LD	2-28 VL-L	2-28 Vrms	3 KHZ-5 KHZ	All Input and Reference voltages are auto ranging
LE	2-28 VL-L	2-28 Vrms	5 KHZ-7 KHZ	All Input and Reference voltages are auto ranging
LF	2-28 VL-L	2-28 Vrms	7 KHZ-10 KHZ	All Input and Reference voltages are auto ranging
LG	2-28 VL-L	2-28 Vrms	10 KHZ-20 KHZ	All Input and Reference voltages are auto ranging
LX	x	x	x	Four channels defined in code table

Note 2: **Synchro/Resolver four channel Measurement module selection:**

(For ranges other than those listed contact factory. Customer should indicate the actual frequency applicable to his design to assure that the correct default band width is set at the factory.

(Code)	Input voltage	Reference voltage	Frequency band	Remarks
SA:	2-28 VL-L	2-115 Vrms	50-400 Hz	All Input and Reference voltages are auto ranging
SB	2-28 VL-L	2-115 Vrms	400 Hz-1 KHZ	All Input and Reference voltages are auto ranging
SC	2-28 VL-L	2-115 Vrms	1 KHZ-3 KHZ	All Input and Reference voltages are auto ranging
SD	2-28 VL-L	2-115 Vrms	3 KHZ-5 KHZ	All Input and Reference voltages are auto ranging
SE	2-28 VL-L	2-115 Vrms	5 KHZ-7 KHZ	All Input and Reference voltages are auto ranging
SF	2-28 VL-L	2-115 Vrms	7 KHZ-10 KHZ	All Input and Reference voltages are auto ranging
SG	2-28 VL-L	2-115 Vrms	10 KHZ-20 KHZ	All Input and Reference voltages are auto ranging
SH	90 VL-L	115 Vrms	50-400 Hz	Four channels
SJ	90 VL-L	115 Vrms	400 Hz- 1 KHZ	Four channels
SX	x	x	x	Four channels defined in code table

Note 3: Encoder/Commutation Option:

Encoder / Commutation Outputs available only for S/Ds installed in Modules 1 and 2 (8 channel max).

REVISION PAGE

Revision	Description of Change	Engineer	Date
1.0	Initial release, based on 78C1 rev 4.0 / Renamed 76C2 / Update memory map and specifications	AS	9/25/06
1.1	Web release	AS	11/29/06