Six (6) LVDT/RVDT Measurement Channels

Encoder & Velocity Outputs, 16 Bit; Continuous Self Test;
Optional On-Board Programmable Excitation Supply
16 Programmable TTL Digital I/O

Typical Configuration Photo

FEATURES

- **Only +5 VDC.**
- 16 bit resolution
- 0.025% FS (Full Scale) Accuracy
- Continuous background testing with Excitation and Signal loss detection
- **Self-calibrating (Does not require removal) Programmable Bandwidth**
- Optional programmable reference excitation
- Two banks of 8 (16 total) TTL Digital I/O - Input/output programmable for each bank.
- Watchdog timer and soft reset
- 360 Hz to 10 KHz
- Galvanic isolation
- Latch feature
- Synthetic reference compensates for ±60° phase shift
- No adjustments or trimming required

Typical Configuration Photo

DESCRIPTION:

This DSP based stack-through PC/104 module offers six (6) separate isolated "PROGRAMMABLE" LVDT/RVDT-to-Digital tracking converters, 16 TTL Digital I/O, extensive diagnostics, and optional Reference. Each channel also produces differential incremental encoder (A&B) outputs (with programmable resolution) and a zero degree marker pulse. Instead of buying cards that are set for specific inputs, the uniqueness of this design makes it possible to order our standard card that auto-ranges between 2.0 and 28 volts. Operating frequency between 360 Hz and 10 KHz can be specified (see part number). Each channel is programmable for either 2 wire or 3, 4 wire inputs. For 2 wire inputs, the output is computed as A/B (where A is the L(R)VDT output and B is the excitation) and is expressed as % of Full Scale (FS). For 3 or 4-wire devices, the output is computed as A-B/A+B and is expressed as % FS. This card uses a derived reference ratiometric design approach that is insensitive to magnitude, temperature, frequency and phase shift effects. The ratiometric technique assures that the output will change only when the L(R)VDT position changes and will ignore excitation voltage variations. The "Latch" feature permits the user to read all channels at the same time. Reading will unlatch that channel. The converters utilize a Type II servo loop processing technique that enables tracking, at full accuracy, up to the specified rate. Intermediate transparent latches, on all data outputs, guarantee that current valid data is always available for any channel without affecting the tracking performance of the converters. The optional on–board excitation is field programmable. Digital velocity outputs, Encoder (A & B) plus Index outputs, are available. Contact factory for detailed information. To simplify logistics, Part number, S/N, Date code, & Rev. are stored in non-volatile memory locations.

DIAGNOSTICS AND BUILT-IN-TEST (BIT):

This board incorporates major diagnostics that offer substantial improvements to system reliability because user is alerted to channel malfunction. Three different tests (one on-line and two off-line) can be selected:

The (D2) test (on-line) is the automatic background Built-In-Test (BIT). Each channel is checked over the programmed Signal range to a measuring accuracy 0.2% FS, and each Signal and Excitation is monitored. Results are available in registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The (D3) test (off-line) if enabled, starts an initiated BIT that disconnects all channels from the outside world and connects them across an internal stimulus that generates and measures multiple voltages to a test accuracy of 0.2% FS. External excitation is not required. Results can be read from registers. The testing requires no external programming and can be initiated or terminated via the bus.

The (D0) test (off-line) is used to check the card and the PC-bus interface. All channels are disconnected from the outside world, allowing user to write any number of input positions to the card and then read the data from the interface. External excitation is not required.

North Atlantic Industries
Apex Signal Division

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SPECIFICATIONS:

LVDT/RVDT Measurement:

(Applies to each channel unless otherwise specified)

Resolution:	16 bit
Accuracy:	0.025% FS
Bandwidth:	40 Hz for 400 – 1 KHz versions. 75 Hz for 1 KHz and above versions (default). Band Width setting is programmable.
Input format:	LVDT or RVDT
Input voltage	Autoranging from 2.0 to 28 Vrms. Galvanic isolation.
Excitation voltage:	2.0 to 115 Vrms.
Input Impedance:	40 KΩ min. at 360 Hz
Frequency:	Specify between 360 Hz to 10 KHz, (See part number (P/N))
Phase shift:	Automatically compensates for phase shifts between the transducer excitation and Output up to ±60° (3 or 4-wire units ignore phase shift)
Encoder outputs:	Either 12,13,14,15, or 16 bit resolution, (programmable) and Index marker. 12 bit resolution is equivalent to 1,024 cycles (4,096 transitions) etc. Differential outputs. The encoder resolution is fixed and does not change with speed. (Optional, see P/N).
Velocity, Digital:	16 bit resolution; Linearity: 0.1%. Scalable to 0.03% of Stroke / Sec resolution.
Wrap around Self Test:	Three powerful test methods are described in the Programming Instructions.
Power:	+ 5 VDC @ 1.25 A (1.75 A peak) plus excitation supply power (if specified)
Temperature, operating:	-40°C to +80°C;
Storage temperature:	-55°C to +105°C.
Conformal coating:	Both sides of the board can be conformal coated (See part number).
Weight:	4 oz.

REFERENCE SUPPLY:

Optional (See part number configurator)

Voltage:	2-28 Vrms, programmable, resolution 0.1 Vrms. Or 115 Vrms fixed. Galvanic isolation.
Accuracy	± 3%
Distortion:	± 2% THD
Frequency:	360 Hz to 10 KHz ±1% with 1 Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	3 VA max. @ 40° min. inductive; 115 mA max @ 26 VAC; 26 mA @ 115 VAC Note: Power (VA) is reduced linearly as the Reference Voltage decreases.
Ground:	Isolated from system ground.

DIGITAL I/O:

TTL and CMOS compatible.

Includes “bus hold”. Therefore, when used as inputs, no external pull-up or pull-down resistors are required.

$V_{out\ L:}$ 0.55 V max. at I_{OL} of 64 mA max.
$V_{out\ H:}$ 2.0 V min. at I_{OH} of 32 mA max.
$V_{out\ H:}$ 3.0 V min. at I_{OH} of 3 mA
$V_{in\ L:}$ 0.8 V
$V_{in\ H:}$ 2.0 V
$V_{in\ max.:}$ 5.0 V

PRINCIPALS OF OPERATION (LVDT): Typically the primary is excited by an ac source, causing a magnetic flux to be generated within the transducer. Voltages are induced in the two secondaries, with the magnitude varying with the position of the core. Usually, the secondaries are connected in series opposition, causing a net output voltage of zero when the core is at the electrical center. When the core is displaced in either direction from center the voltage increases linearly either in phase or out of phase with the excitation depending on the direction.

Interfacing L(R)VDT to Converter:

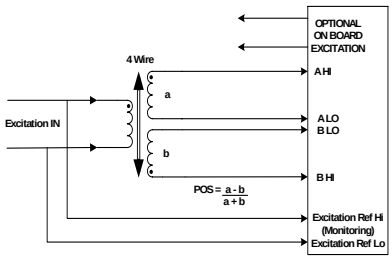
Two common connection methods are:

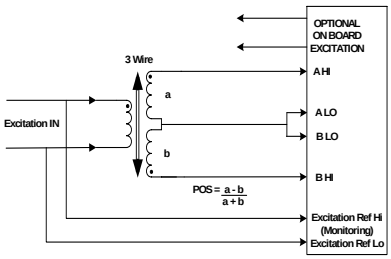
1. Primary as reference (Two-wire L(R)VDT system)
2. Derived reference (Three/four-wire L(R)VDT system)

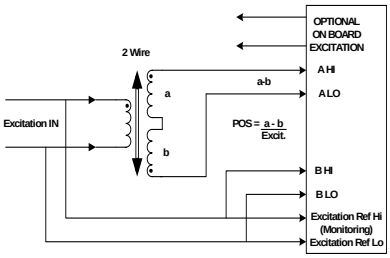
Two-wire system: This method of connection converts the widest range of L(R)VDT sensors and is the most sensitive to excitation voltage variations, temperature and phase shift effects. Measurement is described as the function V_A / V_{EXC} whereby V_A is the L(R)VDT signal output and V_{EXC} is the excitation source. This measurement is provided as a percentage of full scale (%FS).

Three/four-wire L(R)VDT: The L(R)VDT is again excited from the primary side, but the converter reference is the sum of V_A + V_B that has constant amplitude for changing core displacement This system is insensitive to temperature effects, phase shifts and oscillator instability and solves the identity $(V_A – V_B)/(V_A + V_B)$. This measurement is provided as a percentage of full scale (%FS).

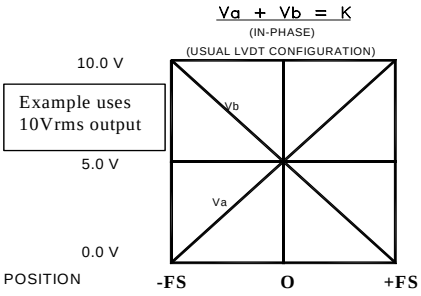
Various L(R)VDT configurations







L(R)VDT Coil Voltage vs. Position



Va+Vb=10V	Va+Vb=10V	Va+Vb=10V
Va-Vb=-10V	Va-Vb=0V	Va-Vb=10V
Va=0V	Va=5V	Va=10V
Vb=10V	Vb=5V	Vb=0V

Two-Wire L(R)VDT Connections:

Connect V_A (or sometimes referred as $V_A – V_B$) L(R)VDT output to Signal A inputs and the Excitation to Signal B inputs. Excitation should also be connected to the Excitation input to enable card to sense and report any excitation loss.

Three or Four-Wire L(R)VDT Connections:

Connect V_A and V_B L(R)VDT outputs to Signal A and B inputs respectively. Excitation is not used, but should be connected to the Excitation input to enable the card to sense and report any excitation loss.

PROGRAMMING INSTRUCTIONS:

I/O CONFIGURATION:

This card requires 32 consecutive addresses in the I/O address space on a 32 byte boundary. The base address is switch settable in the 000-3E0 hex (0 to 992) address range.

ADDRESS= BASE + OFFSET

NOTE: Base addresses to avoid:

378-37F	Parallel Printer Port	3B0-3BF	Monochrome Display	3F8-3FF	Asynch Comm I/O	3F0-3F7	Floppy Disk

Register Bit Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Latch outputs	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X
Active channels	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
TTL Digital I/O	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0
Bank Select	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D0
Status, Excitation	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Signal	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Test	X	X	X	X	X	X	X	X	X	X	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Summary	X	X	X	X	X	X	X	X	X	X	X	X	Test fail	X	Ref. loss	Sig. loss
(A & B) resolution:	**0**	X	X	X	X	X	X	X	X	X	X	X	X	**D2**	**D1**	**D0**

↑ **"0" = Encoder**

↓ **(A & B) resolution:** ↑

	16 bit	0	0	0
	15 bit	0	0	1
	14 bit	0	1	0
	13 bit	0	1	1
	12 bit	1	0	0

Note 1 – values are rounded off.

PAGE SPECIFIC REGISTER MAP:

Page 1 (1E = 0)

00	Position Data 1	R	08	Position Data 5	R	10	Signal scale 1	W/R	18	Signal scale 5	W/R
02	Position Data 2	R	0A	Position Data 6	R	12	Signal scale 2	W/R	1A	Signal scale 6	W/R
04	Position Data 3	R	0C	Not used		14	Signal scale 3	W/R	1C	2-wire/4-wire select	W/R
06	Position Data 4	R	0E	Not used		16	Signal scale 4	W/R	1E	Page Register = 0	W/R

Page 2 (1E = 1)

00	Ch.1 Velocity	R	08	Ch.5 Velocity	R	10	Ch.1 Velocity Scale	W/R	18	Ch.5 Velocity Scale	W/R
02	Ch.2 Velocity	R	0A	Ch.6 Velocity	R	12	Ch.2 Velocity Scale	W/R	1A	Ch.6 Velocity Scale	W/R
04	Ch.3 Velocity	R	0C	Not used		14	Ch.3 Velocity Scale	W/R	1C	Not used	
06	Ch.4 Velocity	R	0E	Not used		16	Ch.4 Velocity Scale	W/R	1E	Page Register =1	W/R

Page 3 (1E = 2)

00	Active channels	W/R	08	Latch	W	10	Status, Signal Loss	R	18	Not used	
02	Test D2 verify	W/R	0A	POST Enable	W/R	12	Status, Excitation Loss	R	1A	Excitation Freq	W/R
04	Test Enable	W/R	0C	Not used		14	Status, Test Fail	R	1C	Excitation Voltage	W/R
06	Test Position	W/R	0E	Not used		16	Status, Summary	R	1E	Page Register = 2	W/R

Page 4 (1E = 3)

00	Not used	08	Not used	10	Ch.1 (A & B) resolution	W/R	18	Ch.5 (A & B) resolution	W/R
02	Not used	0A	Not used	12	Ch.2 (A & B) resolution	W/R	1A	Ch.6 (A & B) resolution	W/R
04	Not used	0C	Not used	14	Ch.3 (A & B) resolution	W/R	1C	Not used	
06	Not used	0E	Not used	16	Ch.4 (A & B) resolution	W/R	1E	Page Register = 3	W/R

Page 5 (1E = 4)

00	Watchdog timer	W/R	08	Date Code	R	10	Not Used	18	Not used
02	Soft reset	W	0A	PCB rev.	R	12	Not used	1A	Not used
04	Part Number	R	0C	DSP rev.	R	14	Not used	1C	Not used
06	Serial Number	R	0E	FPGA rev.	R	16	Not used	1E	Page Register = 4 W/R

Page 6 (1E = 5)

00	0-7 Bank select	W/R	08	Not used		10	Not used	18	Not used
02	8-15 Bank select	W/R	0A	Not used		12	Not used	1A	Not used
04	Output	W	0C	Not used		14	Not used	1C	Not used
06	Input	R	0E	Not used		16	Not used	1E	Page Register = 5 W/R

Page 7 (1E = 6)

00	Ch.1 (A+B) Magnitude	W/R	08	Ch.5 (A+B) Magnitude	W/R	10	Not used	18	Not used
02	Ch.2 (A+B) Magnitude	W/R	0A	Ch.6 (A+B) Magnitude	W/R	12	Not used	1A	Not used
04	Ch.3 (A+B) Magnitude	W/R	0C	Ch.7 (A+B) Magnitude	W/R	14	Not used	1C	Not used
06	Ch.4 (A+B) Magnitude	W/R	0E	Ch.8 (A+B) Magnitude	W/R	16	Not used	1E	Page Register = 6 W/R

Page 8 (1E = 7)

00	Ch.1 Bandwidth	W/R	08	Ch.5 Bandwidth	W/R	10	Not used	18	Not used
02	Ch.2 Bandwidth	W/R	0A	Ch.6 Bandwidth	W/R	12	Not used	1A	Not used
04	Ch.3 Bandwidth	W/R	0C	Bandwidth Select	W/R	14	Not used	1C	Not used
06	Ch.4 Bandwidth	W/R	0E	Not used		16	Not used	1E	Page Register = 7 W/R

Page 9 (1E = 8) (Factory Use Only)

00		08	Not used	10	Not used	18	Not used
02	Not used	0A	Not used	12	Not used	1A	Not used
04	Not used	0C	Not used	14	Not used	1C	Not used
06	Not used	0E	Not used	16	Not used	1E	Page Register = 8 W/R

Page 10 (1E = 9)

00	Ch.1 Freq Lo	R	08	Ch.3 Freq Lo	R	10	Ch.5 Freq Lo	R	18	Not used	
02	Ch.1 Freq Hi	R	0A	Ch.3 Freq Hi	R	12	Ch.5 Freq Hi	R	1A	Not used	
04	Ch.2 Freq Lo	R	0C	Ch.4 Freq Lo	R	14	Ch.6 Freq Lo	R	1C	Not used	
06	Ch.2 Freq Hi	R	0E	Ch.4 Freq Hi	R	16	Ch.6 Freq Hi	R	1E	Page Register = 9	W/R

Page 11 (1E = A)

00	Ch.1 VLL	R	08	Ch.5 VLL	R	10	Ch.3 VExcitation	R	18	Not used	
02	Ch.2 VLL	R	0A	Ch.6 VLL	R	12	Ch.4 VExcitation	R	1A	Not used	
04	Ch.3 VLL	R	0C	Ch.1 VExcitation	R	14	Ch.5 VExcitation	R	1C	Not used	
06	Ch.4 VLL	R	0E	Ch.2 VExcitation	R	16	Ch.6 VExcitation	R	1E	Page Register = A	W/R

Page 12 (1E = B)

00	Ch.1 VLL Loss Thresh	W/R	08	Ch.5 VLL Loss Thresh	W/R	10	Ch.3 ExcV Loss Thresh	W/R	18	Not used	
02	Ch.2 VLL Loss Thresh	W/R	0A	Ch.6 VLL Loss Thresh	W/R	12	Ch.4 ExcV Loss Thresh	W/R	1A	Not used	
04	Ch.3 VLL Loss Thresh	W/R	0C	Ch.1 ExcV Loss Thresh	W/R	14	Ch.5 ExcV Loss Thresh	W/R	1C	Not used	
06	Ch.4 VLL Loss Thresh	W/R	0E	Ch.2 ExcV Loss Thresh	W/R	16	Ch.6 ExcV Loss Thresh	W/R	1E	Page Register = B	W/R

Page 13 (1E = C)

00	L/D SIG STAT INT ENBL	W/R	08	Not Used	10	Not Used	18	Not used	
02	L/D REF STAT INT ENBL	W/R	0A	Not Used	12	Not Used	1A	Not used	
04	L/D BIT STAT INT ENBL	W/R	0C	Not Used	14	Not Used	1C	Not used	
06	Not Used		0E	Not Used	16	Not Used	1E	Page Register = C	W/R

Page 14 (1E = D) (Factory Use Only – “htext”)

00		08		10		18	
02		0A		12		1A	
04		0C		14		1C	
06		0E		16		1E	

Page 15 (1E = E) (Factory Use Only – “htext”)

00		08		10		18	
02		0A		12		1A	
04		0C		14		1C	
06		0E		16		1E	

Page 16 (1E = F) (Factory Use Only – “htext”)

00		08		10		18	
02		0A		12		1A	
04		0C		14		1C	
06		0E		16		1E	

PROGRAMMING DESCRIPTIONS

At Power ON or system reset, all parameters are restored to default setup.

Active Channels
Set the bit, corresponding to each channel to be monitored during BIT testing, in the Active Channel register ("1"=active; "0"=not used). Omitting this step will produce false alarms because unused channels will set faults.

Read Position Data
Read the Position Data Register corresponding to a given channel.

Data Format (2-wire)
The output data is A / B and represents %FS. Format is two's complement. Max. positive excursion is 7FFF, 0 = 0, and max. negative excursion is 8000.

Data Format (4-wire)
The output data is A-B/A+B and represents %FS. Format is two's complement. Max. positive excursion is 7FFF, 0 = 0, and max. negative excursion is 8000.

Latch
Latch the position data for all channels by writing "1" to D1 of Latch register. Reading channel will disengage latch for that channel.

Programming Signal Scale
For two wire applications the **Signal Scale** registers should be set to the Transformation Ratio of the L(R)VDT, so that full scale output code is reached at full travel.

For 3 or 4 wire applications the L(R)VDT has two output voltages referred to as A and B. When connected to the A and B Signal inputs no scaling is required because the inputs are Autoranging, however the signal register can be used to scale the output code.

The default setting for the **Signal Scale** registers are FFFFh. This results in a full scale output Ring for full travel of the L(R)VDT. A full scale output Ring for less then full travel of the L(R)VDT can be programmed by writing to the Signal registers. For example writing 8000h to the **Signal Scale** Register for channel 1 will result in channel 1 having a full scale output Ring for one half travel of the L(R)VDT

(A+B) output magnitude
Read 16 bit word, at appropriate register, and multiply by 0.01 Volt to R the magnitude, of the sum, of signals A & B.

Velocity Scale Factor
To scale the Max Velocity word for 150 Strokes / Second (SpS), set Velocity Scale Factor = 4095 in HEX (max velocity word of 7FFFh being max. CW rotation, and 8000h being max. CCW rotation).
Scaling effects **only** the Velocity output word and not the dynamic performance.

Ex: To get max. velocity word @ 150 SPS: 4095(150/150) = 4095 (0FFFh) This is also the Factory setting.
To get max. velocity word @ 50 SPS. 4095(150/50) = 12,285 (2FFDh)
To get max. velocity word @ 9.375 SPS.4095(150/9.375) = 65,520 (FFF0h) This is also the lowest setting.

Velocity Output
Read Velocity registers of each channel as a 2's complement word, with 7FFFh being max. CW rotation, and 8000h being max. CCW rotation.

When max. velocity is set to 150 SpS, an actual speed of 10 SpS CW would be R as 0888h.
When max. velocity is set to 150 SpS, an actual speed of 10 SpS CCW would be R as F778h.
When max. velocity is set to 50 SpS, an actual speed of 10 SpS CW would be R as 1999h.
When max. velocity is set to 50 SpS, an actual speed of 10 SpS CCW would be R as E667h.

To convert a velocity word, for example E667h, into rps: If max. velocity set to 50 SpS, then
SpS = 50 x E667h / 32,768 = 50 x -6,553 / 32,768 = -10 SpS

2 Wire / 4 Wire Format Select: Write a "1" to the bit corresponding to the channel, to be programmed, for two wire operation. Write a "0" for 3 or 4 Wire operation.

Bandwidth
The bandwidth for each channel is individually programmable when the *Bandwidth Select* register channel is set to "Manual". The minimum BW is 2 Hz, and the maximum BW is 1000 Hz. LSB is 1 Hz. Write desired BW as unsigned integer, between 2 and 1000, to associated channel register. All values greater than 1000 will be processed as 1000 Hz. All values less than 2 will be processed as 2 Hz. When *Bandwidth Select* register channel is set to "Automatic", *Bandwidth* register will report the channel bandwidth.

When in "Manual BW" mode, the user can enter the BW between a range of 2 Hz and 1000 Hz, in 2 Hz increments.

Bandwidth Select
BW Select register sets the "Automatic" or "Manual" Bandwidth control. This register is bitmapped per channel; (i.e. D0 = CH1, D1 = CH2, etc.). "1" indicates automatic bandwidth. "0" indicates manual control.
The Automatic BW feature, when enabled, reads the input reference frequency and automatically adjusts the BW to approximately 1/10 of the carrier frequency. This Auto BW range will be a minimum of 6 Hz with a maximum of 1280 Hz.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1	FUNCTION
BANDWIDTH SELECT	X	X	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D=DATA BIT

Input Reference Frequency Measurement
Each individual channel input reference frequency is measured and the value reported to a corresponding R register. The input reference frequency is reported to a resolution of 0.01 Hz. The output is in integer decimal format. For example, if channel 1 input reference is 400 Hz, the output measurement word from the corresponding register would be 40000.

Input Signal Voltage (VLL) Measurement
Each individual channel input signal voltage "VLL" is measured and the value reported to a corresponding R register. The input voltage is reported to a resolution of 10 mv rms. The output is in integer decimal format. For example, if channel 1 input signal voltage is 11.8 Vrms, the output measurement word from the corresponding register would be 1180.

Input Reference Loss Detection Threshold
Each individual channel input reference voltage is measured. By setting the Input Reference Loss detection threshold, the user has capability of tailoring when reference loss detection is indicated during the D2 background test. The reference loss threshold is set by entering the voltage level in decimal integer format to a resolution of 10 mv. For example, if the user wishes channel 1 reference loss threshold set for 2 Vrms, the register would be set to 200.

Input Signal Loss Detection Threshold
Each individual channel input signal voltage is measured. By setting the Input Signal Loss detection threshold, the user has capability of tailoring when signal loss detection is indicated during the D2 background test. The signal loss threshold is set by entering the voltage level in decimal integer format to a resolution of 10 mv. For example, if the user wishes channel 1 signal loss threshold set for 4 Vrms, the register would be set to 400.

D0 Test Enable
Used to check card and PC interface. Writing "1" to the D0 bit of the *Test Enable Register* disconnects all channels from the outside world, enabling the user to generate any test angle by writing an integer value, to the *Test Angle Register*. Data is then read through the interface (after writing, allow 400 ms before reading). External reference is not required. (e.g. 330° = angle/(360/2^{16})).

Signal and Reference monitoring is disabled during D0 test.

D2 Test Enable
Writing "1" to the D2 bit of the *Test Enable Register* enables the on-line accuracy BIT test status reporting to the *Status, Test BIT Fail* register of all channels set active. Accuracy for each channel is monitored to a test accuracy of 0.2% FS

D3 Test Enable
Writing "1" to the D3 bit of the *Test Enable Register* initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.2% FS. External reference is not required. The test cycle is completed within 45 seconds and results can be read from the *Test Status Registers* when D3 bit changes from "1" to "0" The testing can be terminated at any time by writing "0" to D3 bit of the *Test Enable Register*.

Signal and Reference monitoring is disabled during D3 test.

Status, Test (Fail)
Check the channel's corresponding bit of the *Test Status Register* for status (accuracy BIT) for each active channel. A "0" means accuracy passes; A "1" indicates a failure on an active channel. Channels that are inactive are also set to "0". (Test cycle takes 45 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the *Test Status Register*. Reading will unlatch register.

Status, Reference (Loss)
Check the channel's corresponding bit of the *Reference Status Register* for status of the reference input for each active channel. A "1" means Reference LOSS, a "0" means Reference valid or "OK" (as compared with value set in *Reference Loss Detection Threshold* register) on active channels. Channels that are inactive are also set to "0". (Reference loss is detected within 2 seconds). Any Reference status failure, transient or intermittent will latch the *Reference Status Register*. Reading will unlatch register.

This register also corresponds with the *Input Reference Loss Detection Threshold Register.*

Status, Signal (Loss)
Check the corresponding bit of the *Signal Status Register* for status of the input signals for each active channel. A "1" means Signal "LOSS" (level compared with value set in *Signal Loss Threshold* register), a "0" means Signal loss on active channels. Channels that are inactive are also set to "0". (Signal loss is detected after 2 seconds). Any signal status failure, transient or intermittent will latch the *Signal Status Register*. Reading will unlatch register.
Now, let us consider what happens when a status bit changes before registers are read. For example, if a reference loss was detected and latched into registers and subsequent scans find that the reference was reconnected, then this status change will be held in background until registers are read. Within 250ms, registers will be updated with the background data. Allow 250 ms to scan all channels.

This register also corresponds with the *Input Signal Loss Detection Threshold Register.*

Status, Summary
Monitoring a change due to a problem/failure can be accomplished by polling the *Summary Status Register.* By reading the *Summary Status Register*, the user can determine whether a change occurred from Signal Loss, Reference Loss, or Test Accuracy Error. To determine which channel was affected, read the appropriate register. Any status failure, transient or intermittent will latch the *Summary Status Register*. Reading will unlatch register.

Optional (A&B) Encoder Resolution
To set Encoder Mode, write a "0" to the D15 bit and the appropriate code for the desired resolution to the D2, D1 & D0 bits of the corresponding channel to the (*A&B) Resolution/Poles Register*. Changing the resolution for any channel can be done on the fly. The default is a 12bit resolution encoder output.

Note: Encoder/Commutation outputs are optional; see part ordering information.

Optional Commutation Outputs (A, B, C)
To set Commutation Mode, write a "1" to the D15 bit and the appropriate code for the required motor poles to the D2, D1 & D0 bits of the corresponding channel to the *(A&B) Resolution/Poles Register*. See Register Bit map table.
Note: Encoder/Commutation outputs are optional; see part ordering information.

Reference Supply (OSC) (Optional)
For frequency, write a 16-bit word (Ex: 400 Hz = 0x190) to OSC Frequency Register. For voltage, write a word (Ex: 26.1Vrms = 0x105) with LSB = 0.1Vrms, to OSC Voltage Register. It is recommended that user program the required frequency before setting the output voltage.

DIGITAL I/O FUNCTIONS

Bank Select for Digital I/O's
Controls the direction of each bank of 8, Digital I/O. A "0" in a Bank Select Register sets the corresponding bank to be Inputs. A "1" sets the bank to be Outputs.

Input Register
Indicates the logic state of Digital I/O bits. Upper byte represents bank 8-15, lower byte represents bank 0-7.

Output Register
Controls the logic state of Digital I/O's, when bank is set to be Outputs. Upper-byte controls bank 8-15; lower byte controls bank 0-7.

ADDITIONAL FUNCTIONS

Soft Reset
Writing a "1" (Level sensitive) to the Soft Reset Register initiates and holds software in reset state. Then, writing "0" initiates reboot (takes 400 ms). Following the soft reset, a power on automatic calibration test is run and completes in approximately 30 seconds. This function is equivalent to Power on Reset.

Watchdog Timer
This feature monitors the *Watchdog Timer Register*. When it detects that a code has been received, that code will be inverted within 100 µsec. The inverted code stays in the register until replaced by a new code. The user should look for the inverted code, after 100 µsec, to confirm that the processor is operating.

Part Number
Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

Serial Number
Read as a 16-bit binary word from the *Serial Number Register*. This is the serial number of that particular board.

Date Code
Read as decimal number from the *Date Code Register*. Four digits represent YYWW (Year, Year, Week, Week)

Rev Levels
There are a total of 3 *Revision Level Registers*, which are listed below. Each register is defined as 16 bits. The integer value of that particular register corresponds to the actual revision.

Rev level PCB
Rev level DSP
Rev level FPGA

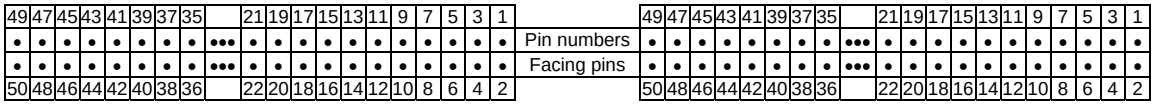
CONNECTORS:

JP6: AMP 104130-9, Mate: AMP 1-746285-0 & strain relief 499252-4

Pin		Pin		Pin		Pin		Pin		Pin		Pin	
1	Ch.3 - BHi	9	Ground	17	D I/0 4	25	Ch.1 - AHi	33	Ch.3 Sig B Lo	41	Ch.2 Sig A Lo	49	Ch.1 Sig B Hi
2	Ch.3 - BLo	10	Ground	18	D I/0 5	26	Ch.1 - ALo	34	Ch.3 Sig A Lo	42	Ch.2 Sig A Hi	50	Ch.2 Exc. Hi
3	Ch.3 - ALo	11	Ch.3 - IDXHi	19	D I/0 6	27	Ch.1 - BHi	35	Ch.3 Exc. Lo	43	Ch.1 Sig A Hi		
4	Ch.3 - AHi	12	Ch.3 - IDXLo	20	D I/0 7	28	Ch.1 - BLo	36	Ch.3 Exc. Hi	44	Ch.1 Sig A Lo		
5	Ch.2 - IDXHi	13	D I/0 0	21	Ch.1 - IDXHi	29	Ground	37	Exc. Lo Out	45	Ch.2 Sig B Hi		
6	Ch.2 - IDXLo	14	D I/0 1	22	Ch.1 - IDXLo	30	Ground	38	Ch.1 Exc. Lo	46	Ch.2 Sig B Lo		
7	Ch.2 - BLo	15	D I/0 2	23	Ch.2 - AHi	31	Ch.3 Sig B Hi	39	Exc. Hi Out	47	Ch.1 Sig B Lo		
8	Ch.2 - BHi	16	D I/0 3	24	Ch.2 - ALo	32	Ch.3 Sig A Hi	40	Ch.1 Exc. Hi	48	Ch.2 Exc. Lo		

JP7: AMP 104130-9, Mate: AMP 1-746285-0 & strain relief 499252-4

Pin		Pin		Pin		Pin		Pin		Pin		Pin	
1	Ch.6 Sig B Lo	9	Ch.5 Sig A Hi	17	Ch.4 Exc. Lo	25	Ch.4 - IDXHi	33	Ch.6 - AHi	41	D I/0 8	49	Ground
2	Ch.6 Exc. Lo	10	Ch.5 Exc. Hi	18	Ch.4 Sig B Lo	26	Ch.4 - IDXLo	34	Ch.6 - ALo	42	D I/0 9	50	Ground
3	Ch.5 Sig B Lo	11	Ch.6 Sig A Lo	19	Ground	27	Ch.5 - AHi	35	Ch.6 - BHi	43	D I/0 10		
4	Ch.6 Exc. Hi	12	Ch.4 Sig A Hi	20	Ground	28	Ch.5 - ALo	36	Ch.6 - BLo	44	D I/0 11		
5	Ch.5 Sig B Hi	13	Ch.6 Sig A Hi	21	Ch.4 - AHi	29	Ch.5 - BHi	37	Ch.6 - IDXHi	45	D I/0 12		
6	Ch.6 Sig B Hi	14	Ch.4 Sig A Lo	22	Ch.4 - ALo	30	Ch.5 - BLo	38	Ch.6 - IDXLo	46	D I/0 13		
7	Ch.5 Sig A Lo	15	Ch.4 Exc. Hi	23	Ch.4 - BHi	31	Ch.5 - IDXHi	39	Ground	47	D I/0 14		
8	Ch.5 Exc. Lo	16	Ch.4 Sig B Hi	24	Ch.4 - BLo	32	Ch.5 - IDXLo	40	Ground	48	D I/0 15		



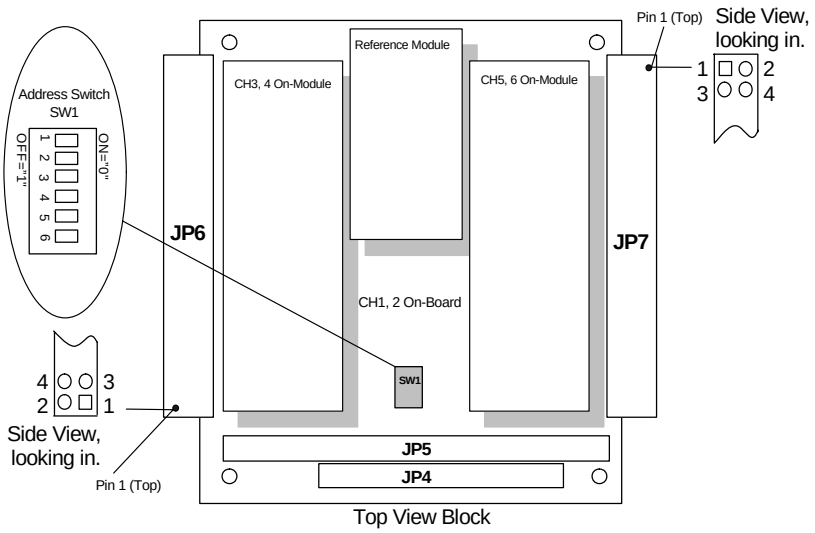
NOTES:

1. Optional Reference output is NOT internally tied to individual channel reference inputs.
2. Do not connect to any undesignated pins.
3. When commutation outputs (A, B, C) are selected Index+ becomes C+ and Index- becomes C-.
4. Pins JP5-B10 and JP4-C20 have been removed for keying purposes.
5. Connector pin-out nomenclature:

Examples:	
L(R)VDT signals	Ch.x Sig A Hi
Encoder/Commutators	Ch.x - AHi
Digital I/O	D I/O x

MECHANICAL:

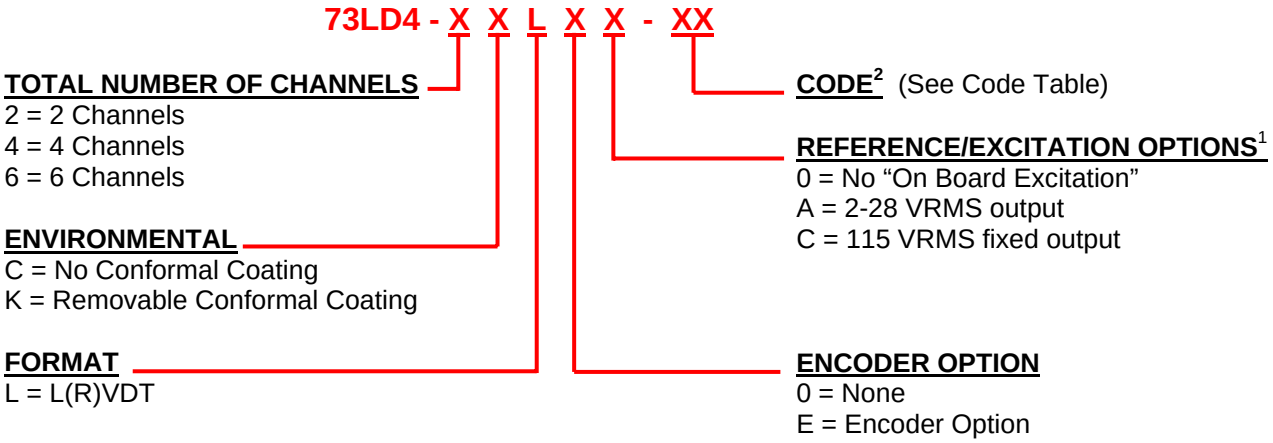
PC/104, Basic Layout



Top View Block

PART NUMBER

PART NUMBER DESIGNATION



Code List:

01	400 HZ
02	2000 HZ
03	3000 HZ
04	5000 HZ
05	7000 HZ
06	2500 HZ

(Contact factory for code list addendum descriptions of code 50 and above)

Notes:

1. On-Board Reference **IS** independent output (not connected internally to any S/D channels).
2. Contact Factory for code list addendum for descriptions of code 50 and above.

Revision Page

Revision	Description of Change	Engineer	Date
1.0	Preliminary Release: Based on 73LD3 rev 5.2; Extended programming capability not added	FH/as	4/18/06
1.2	Added extended programming capability (rev 1.1 skipped)	FH/as	5/11/06
1.3	Added photo to page 1	FR	9/12/06
1.4	Added individual latch function and board ready to register map page 3, 0Ah and 0Ch respectively (pg 8)	AS	2/1/07
1.5	Changed “Discrete” reference to “TTL Digital I/O”; NAI Address update	AS	5/8/07
1.6	Part Number Designation reverts back to “LD3”	AS	6/1/07
A	Initial Release to Agile	AS	12/12/07
A2	Minor corrections / Re-release to Agile (rev A1 skipped)	AS	3/25/08
A3	Re-release to Agile / Clarified module slots and address switch layout	AS	3/28/08