PMC

Eight (8) SYNCHRO/RESOLVER-to-DIGITAL

TO COMMERCIAL OR MILITARY SPECIFICATIONS

FEATURES:

- **Requires ONLY +5 VDC**
- 16-bit resolution for single-speed (up to 24 bits for two-speed configuration)
- ±1 arc-minute accuracy
- Continuous background BIT testing with Reference and Signal loss detection
- **Self-calibrating. Does not require removal for calibration**
- **Synchro/Resolver programmable per channel**
- **Bandwidth programmable per channel up to 1200 Hz**
- Programmable 2-speed ratios: 2 to 255
- 400 Hz to 10 kHz operation
- Tracking rate to 300 rps (18,000 rpm)
- Power-On Self-Test (POST)
- Accurate Digital Velocity outputs
- Watchdog timer and soft reset
- **Automatically supports either 5 V or 3.3 V PCI Bus**
- Synthetic reference compensates for ±60° phase shift
- No adjustments or trimming required
- Part number, S/N, Date Code and Revision in non-volatile memory

DESCRIPTION:

This high density intelligent DSP-based card incorporates eight (8) single-speed or four (4) two-speed tracking converters with extensive diagnostics, and digital velocity outputs. Unique programmability permits user to set each channel for either Synchro or Resolver Input **AND to set the desired bandwidth per channel.** This capability is most desirable for motor control applications because it gives the user total control over one of the loop characteristics.

Any combination of two-speed and single-speed channels can be field programmed to any ratio between 2 and 255. For 2-speed usage, ambiguity circuits maintain monotonic outputs by compensating for misalignment between the Coarse and Fine Synchros. However, the processor will set a flag when it senses that the maximum allowable misalignment of 90°/gear ratio is exceeded. Channels 1-6 have separate reference inputs. Channels 7 & 8 are common because some Jn4 may only use 46 pins.

This card, even when large accelerations are encountered, never looses tracking, because it incorporates the unique capability to automatically shift to higher bandwidths. The shifting is smooth and continuous with no glitches. Tracking rates are only limited to bandwidth restrictions, up to 300 RPS, at 16-bit resolution. **Here again, the high tracking rate and variable bandwidth enables the converters to handle high speeds and acceleration**. The use of Type II servo loop processing techniques enables tracking, at full accuracy, up to the specified rate. A step input will not cause any hang-up condition. Intermediate transparent latches, on all angle and velocity outputs, assure that valid data is always available without interrupts or waiting time. Our synthetic reference compensates for ±60° phase shifts, thus eliminating the need for individual compensation networks. Each channel can be specified for a different voltage or frequency. A watchdog timer is provided to monitor the processor. Part number, S/N, Date Code and Revision are stored in non-volatile memory.

This board incorporates major diagnostics that offer substantial improvements to system reliability, because the user is alerted to channel malfunction. This approach reduces bus traffic, because the Status Registers need not be constantly polled. Three different tests, one on-line and two off-line, can be selected:

The (D2) Test initiates automatic background BIT testing. Each channel is checked every 5° to a testing accuracy of 0.05° and each Signal and Reference is always monitored. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled via the bus.

The (D3) Test initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. Results can be read

from registers and external reference is not required. Any failure triggers an Interrupt (if enabled). The testing requires no external programming, and can be initiated or stopped via the bus.

The (D0) Test is used to check the card and the VME interface. All channels are disconnected from the outside world, allowing the user to write any number of input angles to the card and then to read the data from the interface. External reference is not required.

SPECIFICATIONS:

Resolution:	16 bits (up to 24 bits for two-speed configuration)
Accuracy:	±1 arc-minute
Tracking Rate:	150 RPS max. is standard with normal band width
Bandwidth:	Standard is 40 Hz at 400 Hz, and 100 Hz above 1 kHz. Can be programmed in field From 5 Hz to 1200 Hz per channel.
Input format:	Synchro or Resolver programmable
Gear ratio:	Each channel pair is programmable from 2 to 255
Input voltage:	2-28 V_{L-L}, Autoranging, or 90 V_{L-L}
Input Impedance:	40 kΩ min. for low voltage, 100 kΩ min. for 90 v units
Reference:	2-28 Vrms, Autoranging. Or 115 Vrms
Reference Zin	100 kΩ min.
Frequency:	60 Hz to 10 kHz (see part number)
Phase shift:	The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°.
Velocity, Digital:	16-bit resolution; Linearity: 0.1%. Scalable to 0.1°/sec resolution. BW is same as Signal BW.
Wrap around Self Test:	The three different powerful test methods are detailed in the Description section and further described in the Programming Instructions.
Interrupts:	One Interrupt capability is implemented.
Signal logic levels:	Automatically supports either 5 V or 3.3 V PCI Bus
Power:	+ 5 VDC 1.0 A for 8 channels;
Temperature, operating:	"C" =0°C to +70°C, "E" =-40°C to +85°C (See part number)
Storage temperature:	-55°C to +95°C.
Conformal coating:	Both sides of the board can be conformal coated (see part number).
Weight:	10 oz.

PROGRAMMING INSTRUCTIONS:

MEMORY MAP

000	Ch.1 Data Hi	r	40	Ratio Ch 2/ Ch 1	r/w	CC	Velocity, scale Ch.1	r/w	118	Date code	r
004	Ch.2 Data Hi	r	44	Ratio Ch 4/ Ch 3	r/w	D0	Velocity, scale Ch.2	r/w	11C	Rev. Level, PCB	r
008	Ch.3 Data Hi	r	48	Ratio Ch 6/ Ch 5	r/w	D4	Velocity, scale Ch.3	r/w	120	Rev. Level, Software	r
00C	Ch.4 Data Hi	r	4C	Ratio Ch 8/ Ch 7	r/w	D8	Velocity, scale Ch.4	r/w	124	Rev. Level, Interface FPGA	r
010	Ch.5 Data Hi	r	74	Active channels,	r/w	DC	Velocity, scale Ch.5	r/w	128	Rev. Level, FPGA	r
014	Ch.6 Data Hi	r	78	Test (D2) verify	r/w	E0	Velocity, scale Ch.6	r/w	150	Band width Ch.1	r/w
018	Ch.7 Data Hi	r	7C	Test Enable	r/w	E4	Velocity, scale Ch.7	r/w	154	Band width Ch.2	r/w
01C	Ch.8 Data Hi	r	80	Status, Sig.	r	E8	Velocity, scale Ch.8	r/w	158	Band width Ch.3	r/w
20	Vel.1	r	84	Status, Ref	r	F0	Ch.2 Data Lo	r	15C	Band width Ch.4	r/w
24	Vel.2	r	88	Status, Test,	r	F4	Ch.4 Data Lo	r	160	Band width Ch.5	r/w
28	Vel.3	r	8C	Latch	w	F8	Ch.6 Data Lo	r	164	Band width Ch.6	r/w
2C	Vel.4	r	90	Test angle	w	FC	Ch.8 Data Lo	r	168	Band width Ch.7	r/w
30	Vel.5	r	98	Interrupt enable	r/w	108	Watchdog timer	r/w	16C	Band width Ch.8	r/w
34	Vel.6	r	9C	Interrupt status	r	10C	Soft reset	w			
38	Vel.7	r	A0	Synchro/Resolver	r/w	110	Part #	r			
3C	Vel.8	r	A8	Two Speed Lock-Loss	r/w	114	Serial #	r			

Register Bit Map

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data	180	90	45	22.5	11.2	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0
Synchro/Resolver	X	X	X	X	X	X	X	X	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Test	X	X	X	X	X	X	X	X	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Reference	X	X	X	X	X	X	X	X	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status, Signal	X	X	X	X	X	X	X	X	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Active channels	X	X	X	X	X	X	X	X	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Enable/Status	X	X	X	X	X	X	X	X	X	X	X	X	Test fail	X	Ref.	Sig.
Two-speed lock loss	X	X	X	X	X	X	X	X	X	Ch7/8	X	Ch5/6	X	Ch3/4	X	Ch1/2

INTERRUPT ENABLE & STATUS REGISTERS

#1 = S/D Signal Loss #2 = S/D Reference Loss #4 = S/D Test Accuracy Error

At **Power-ON** or **System Reset**, all parameters are restored to their default condition.

Enter Active Channels: Set the bit corresponding to each channel to be monitored during BIT testing in the Active Channel Register. "1"=active; "0"=not used. Omitting this step will produce false alarms, because unused channels will set faults.

Synchro/Resolver: Set each channel to desired format. '1'= Synchro; '0'=Resolver. Default is '0'

Ratio: Enter the desired ratio, as an integer number, in the *Ratio Register* corresponding to the pair of channels to be used for a two-speed channel. Example: Single speed = 1; 36:1 = integer 36.

Read: For single speed applications (Ratio=1), read individual channels 1,2,3,4,etc. For two-speed applications, read only channels (2,4,6,8,etc.) for the combined output of 16 bits. For resolution up to 24 bits, read Data Lo word, then Data Hi word. Data Lo word, when read, latches Hi word.

In two-speed S/D applications, the single speed information (coarse) from the synchro should be connected to the odd channel of the pair. The N-speed information (multi-speed, fine) from the synchro should be connected to the even channel of the pair. The pairs are defined as: CH1 & 2, CH3 & 4,… CH15 & 16.

Bandwidth: Set each channel with a 16 bit word from 5 to 1200 Hz. LSB = 1 Hz. Default is 40 Hz signal bandwidth at 400 Hz reference, or 100 Hz signal bandwidth for references above 1 kHz.

Two-Speed Lock-Loss: When two Synchros are geared to each other, either electrically or mechanically, in order to achieve higher accuracy, the misalignment of the Coarse and Fine Synchros must not exceed 90°/gear ratio or the digital angle output may not be valid. Should this problem occur, with a given channel pair, the corresponding bit in the *Two-Speed Lock-Loss Register* will be set to "0".

Velocity Output: Read Velocity Registers of each channel as a 2's complement word, with 7FFFh being maximum CW rotation, and 8000h being maximum CCW rotation.

When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CW would be read as 0863h.
When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CCW would be read as F79Ch.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CW would be read as 192Ah.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CCW would be read as E6D5h.

To convert a velocity word to RPS: **Velocity in RPS = Maximum x Output / Full Scale**

If Velocity Output were E6D5h, and maximum velocity were 50.8626 RPS, then
Velocity in RPS = 50.8626 x E6D5h / 32,768 = 50.8626 x -6,442 / 32,768 = -10 RPS

Velocity Scale Factor: The velocity scale factor is used to achieve a greater resolution at lower rotational speeds (RPS). The scale factor is: **4095(152.5878RPS/max RPS),** where the max RPS is selected by the user to achieve the maximum resolution for a desired RPS. Enter the scale factor as an integer to the corresponding *Velocity Scale Register* for that particular channel.

To scale the Max Velocity word for 152.5878 RPS, set Velocity Scale Factor = 4095 (max velocity word of +32,767 (7FFFh) being 152.5878 RPS for CW rotation, and –32,768 (8000h) being 152.5878 RPS for CCW rotation). Scaling effects only the Velocity output word and not the dynamic performance.

To get a maximum velocity word (32,767) @ 152.5878 RPS, Scale Factor = 4095(152.5878/152.5878) = 4095 = 0FFFh;
This results in a velocity resolution of: (152.5878 RPS/32,767) x 360°/RPS = 1.676°/sec (factory default)

To get a maximum velocity word (32,767) @ 50.8626 RPS, Scale Factor = 4095(152.5878/50.8626) = 12,285 = 2FFDh);
This is a velocity resolution of: (50.8626 RPS/32,767) x 360°/RPS = 0.5588°/sec

For 9.5367 RPS max, Scale Factor = 4095(152.5878/9.5367) = 65,520 = FFF0h; 0.10477 °/sec resolution (lowest setting)

D2 Test Enable: Writing "1" to the D2 bit of the *Test Enable Register* initiates automatic background BIT testing that checks each channel every 5° to a test accuracy of 0.05°. The result of an accuracy error is available in the *Test Status Register* and if enabled, an interrupt will be generated (See *Interrupt Register*). A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled. The card will write 55h to the *Test (D2) Verify Register*, every 30 seconds, when the D2 Test is enabled. User can periodically clear the *Test (D2) Verify Register* by writing 00h, waiting 30 seconds, then reading the register again to verify that background BIT testing is activated.

In addition, each S/D Signal and Reference input is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *Signal* and *Reference Status Registers*.

D3 Test Enable: Writing "1" to D3 of *Test Enable Register* initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. External reference is not required. Test cycle is completed within 45 seconds and results can be read from the *Test Status Registers*when D3 changes from "1" to "0" and if enabled, an interrupt will be generated if a BIT failure is detected (See *Interrupt Register*), The testing requires no external programming, and can be terminated at any time by writing "0" at D3 of the *Test Enable Register*.

Signal and Reference monitoring is disabled during the D3 test.

D0 Test Enable: Checks card and interface. Writing "1" to the D0 bit of the *Test Enable Register* disconnects all channels from the outside world and connects them to internal test signals, enabling the user to generate any test angle by writing an integer value, to the *Test Angle Register*, Data is then read through the interface (after writing, allow 400 ms before reading). External reference is not required. (e.g. 330° = angle/(360/2^{16})).

Signal and Reference monitoring is disabled during D0 test.

Status, Test: Check the channel's corresponding bit of the *Test Status Register* for status of BIT testing for each active channel. A "1" means accuracy passes; A "0" indicates a failure on an active channel. Channels that are inactive are also set to "0". (Test cycle takes 45 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the *Test Status Register*. Reading will unlatch register.

Status, Ref: Check the channel's corresponding bit of the *Reference Status Register* for status of the reference input for each active channel. A "1" means Reference ON, a "0" means Reference Loss on active channels. (Reference loss is detected within 2 seconds). Channels that are inactive are also set to "0". Reference monitoring is disabled during D3 or D0 Test. Any Reference status failure, transient or intermittent will latch the *Reference Status Register*. Reading will unlatch register.

Status, Sig: Check the corresponding bit of the *Signal Status Register* for status of the input signals for each active channel. A "1" means Signal is valid (level must be a minimum of 2V), a "0" means Signal loss on active channels. (Signal loss is detected after 2 seconds). Channels that are inactive are also set to "0". Signal monitoring is disabled during D3 and D0 test. Any Signal status failure, transient or intermittent will latch the *Signal Status Register*. Reading will unlatch register.

Now, let us consider what happens when a status bit changes before registers are read. For example, if a reference loss was detected and latched into registers and subsequent scans find that the reference was reconnected, then this status change will be held in background until registers are read. Within 250ms, registers will be updated with the background data. Allow 250 ms to scan all channels.

Soft Reset: (Level sensitive): Writing a "1" initiates and holds software in reset state. Then, writing "0" initiates reboot (takes 400 ms). This function is equivalent to a power-on reset and all registers are cleared.

Watchdog Timer: This feature monitors the Watchdog Timer Register. When it detects that a code has been received, that code will be inverted within 100 µSec. The inverted code stays in the register until replaced by a new code. User, after 100 µSec, should look for the inverted code to confirm that the processor is operating.

Interrupt Registers: Interrupts can be enabled to relay specific problems/failures detected by the card. The problem/failures that generate these interrupts are:

S/D Signal Loss, S/D Reference Loss, S/D Test Accuracy Error,

Each external interrupt can be enabled individually. This is accomplished by writing a "1" to the bit corresponding to desired interrupts to the *Interrupt Enable Register* and a "0" to disable those interrupts not used. Refer to Register Bit Map.

Interrupt Status Registers: When an interrupt is initiated via a problem/failure, the *Interrupt Status Register* can be interrogated by a read to identify, which interrupt occurred. Refer to Table 3. Register is latched when interrupt is generated and unlatched when read.

Note: This register is typically read and cleared by the device driver. Subsequent readings of this register will give clear status.

Part Number: Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned for each part number.

Serial Number: Read as a 16-bit binary word.

Date Code: Read as a decimal number. The four digits represent YYWW (Year,Year,Week,Week)

Rev Levels: Read as a 16 bit binary word. The integer value of the particular register corresponds to the actual rev.

Software - PCI Programming

This section provides programmers the information needed for developing drivers other than those supplied. The following information resides in the PCI configuration registers:

Device ID = 7402h
Vendor ID = 15ACh
Rev = 01h
Subsystem ID = 000115ACh
Base Address = Assigned by the PCI BIOS. Interrogate the PCI BIOS for this information.
Required Address space = 1K for each card.

Connector J5 (Front Panel) SCSI 68 pin.

Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description
37	S1 Ch.1	52	S1 Ch.2	60	S1 Ch.3	67	S1 Ch.4	27	S1 Ch.5	23	S1 Ch.6	19	S1 Ch.7	13	S1 Ch.8
40	S2 Ch.1	51	S2 Ch.2	59	S2 Ch.3	64	S2 Ch.4	34	S2 Ch.5	22	S2 Ch.6	18	S2 Ch.7	12	S2 Ch.8
38	S3 Ch.1	50	S3 Ch.2	58	S3 Ch.3	68	S3 Ch.4	29	S3 Ch.5	24	S3 Ch.6	20	S3 Ch.7	14	S3 Ch.8
39	S4 Ch.1	49	S4 Ch.2	57	S4 Ch.3	63	S4 Ch.4	33	S4 Ch.5	21	S4 Ch.6	17	S4 Ch.7	11	S4 Ch.8
35	RHi Ch.1	48	RHi Ch.2	56	RHi Ch.3	66	RHi Ch.4	31	RHi Ch.5	26	RHi Ch.6	15	RHi Ch.7	15	RHi Ch.8
36	RLo Ch.1	47	RLo Ch.2	55	RLo Ch.3	65	RLo Ch.4	32	RLo Ch.5	25	RLo Ch.6	16	RLo Ch.7	16	RLo Ch.8

Connector Jn 4

Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description
1	S1 Ch.1	7	S1 Ch.2	13	S1 Ch.3	19	S1 Ch.4	25	S1 Ch.5	31	S1 Ch.6	37	S1 Ch.7	43	S1 Ch.8
2	S2 Ch.1	8	S2 Ch.2	14	S2 Ch.3	20	S2 Ch.4	26	S2 Ch.5	32	S2 Ch.6	38	S2 Ch.7	44	S2 Ch.8
3	S3 Ch.1	9	S3 Ch.2	15	S3 Ch.3	21	S3 Ch.4	27	S3 Ch.5	33	S3 Ch.6	39	S3 Ch.7	45	S3 Ch.8
4	S4 Ch.1	10	S4 Ch.2	16	S4 Ch.3	22	S4 Ch.4	28	S4 Ch.5	34	S4 Ch.6	40	S4 Ch.7	46	S4 Ch.8
5	RHi Ch.1	11	RHi Ch.2	17	RHi Ch.3	23	RHi Ch.4	29	RHi Ch.5	35	RHi Ch.6	41	RHi Ch.7	41	RHi Ch.8
6	RLo Ch.1	12	RLo Ch.2	18	RLo Ch.3	24	RLo Ch.4	30	RLo Ch.5	36	RLo Ch.6	42	RLo Ch.7	42	RLo Ch.8

JN4 pins are always active. When front panel connector J5 is specified, both J5 and Jn4 are in parallel.

Code	Format	Input	Ref.	Freq.	Comments
01	Synchro	11.8 (V_{L-L})	26	400	
02	Synchro	90 (V_{L-L})	115	400	
03	Synchro	90 (V_{L-L})	115	60/400	
04	Synchro/Resolver	2-28 (V_{L-L})	2-28	400 Hz to 10 kHz	
05	Resolver	2-28 (V_{L-L})	2-28	400 Hz to 10 kHz	
50	Synchro (Ch. 1,2 & 3) Synchro (Ch. 4)	11.8 (V_{L-L}) 90 (V_{L-L})	26 115	400 400	
52	Resolver 1-8	2-28 (V_{L-L})	2-28	400 Hz to 10 kHz	Ch 1-6 have individual references. Ch 7 & 8 have a common ref.

PART NUMBER DESIGNATION

74SD2 - XX X X 0 - XX

TOTAL NUMBER OF CHANNELS

04 = 4 Channels
08 = 8 Channels

ENVIRONMENTAL

C = 0°C to +70°C
E = -40°C to +85°C
H = E With Removable Conformal Coating
K = C With Removable Conformal Coating

MECHANICAL

F = Front Panel I/O and rear connector I/O
P = Rear connector I/O only

CODE (See Code Table)

Revision Page

Revision	Description of Change	Engineer	Date
A	Initial Release	FH	9/9/33
A2.0	Device ID is 7402	GS	10/16/3
A2.1	Temp range "C" =0°C to +70°C, "E" =-40°C to +85°C (See part number)	GS	11/17/3
A2.2	Galvanic Isolation removed from feature list	GS	2/4/4
A2.3	Adds Code 05	GS	2/12/4
A2.4	Corrected 2-speed 24-bit description; read data Lo first, latches Hi, read data Hi	AS	02 DEC 05