MULTI-FUNCTION CARD

VME and/or 10/100/1000 Base-T Gigabit copper ETHERNET

A/D, D/A, Discrete I/O, TTL I/O, Differential I/O, RTD, Synchro/Resolver and LVDT/RVDT

EXTENSIVE DIAGNOSTICS

FOR COMMERCIAL AND MILITARY APPLICATIONS

Photo – Typical Configuration (heatsink removed for clarity)

FEATURES

- Control either via **VME or Ethernet** port
- **Multiple functions** on a single slot VME card
- Background Self Test
- Geographical addressing (Field selectable)
- Connections via Front panel, P2 / P0 or both
- Conduction cooled versions available

DESCRIPTION

This second generation multi-function card adds Ethernet capability, offers additional programmability, and faster operating speed. As a universal design, it eliminates the need for specialized, single function cards by providing a broad assortment of I/O, Synchro / Resolver and LVDT functions on one single card that can be **controlled either via the VME or via a 10 / 100 / 1000 Base-T Gigabit Copper Ethernet** port.

The "mother board" contains **6 independent module slots**, each of which can be populated with a function specific module. The available functions are as follows:

Function	Module	Channels	Details
A/D	C1, C2, C4, C3	10	±1.25 to ±10, ±40, ±50 VDC and 4-20ma versions
D/A	J3, J5, F3, F1	10	±1.25, ±2.5, ±5V, ±10 VDC, Isolated or Non-Isolated versions
D/A (High voltage)	J8	4	±20 to ±80 VDC, Isolated
D/A (High current)	F5	4	±20 VDC at 100 ma max, Isolated
Signal Generator	E5	4	Function Generator, 10-130kHz, 0-15Vpp (5.3 Vrms)
Digital I/O	D7	16	TTL (5V or 3.3V System Logic Supply), Programmable for Input or Output
	D8	11	Differential Multi-Mode Transceivers
Discrete I/O	K6	16	Discrete (0-80 VDC), Programmable for Input or Output,
LVDT/RVDT	L*	4	LVDT-to-Digital, 2, 3 or 4 wire LVDT and one optional 5 VA excitation
Reference	W1	1	2.2 VA programmable. 2-115 Vrms, 50 Hz-10 KHz,
RTD	G4	6	2, 3 or 4 wire Platinum Resistance Temperature Device Measurement
S/D	S*	4	Synchro/Resolver-to-Digital and one optional 5 VA reference

*indicates wide selection (see part number)

Automatic background BIT testing, an important feature is always enabled and continually checks the health of each channel. There is no need to guess or make assumptions about system performance. A fault is immediately reported and the specific channel is identified. This capability is of tremendous benefit because it identifies and reports a failure, without the need to shut down the equipment for troubleshooting. Testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card and can be disabled on a per channel basis. (See Operational Instructions for further detail within this specification.)

SOFTWARE SUPPORT

The VxWorks Software Support Kit (SSK) is supplied with all VME platform based board level products. This platform's SSK contents include html format help documentation which defines board specific library functions and their respective parameter requirements. A board specific library and its source code is provided (module level c and header files) to facilitate function implementation independent of user operating system (O/S). Portability files are provided to identify Board Support Package (BSP) dependent functions and help port code to other common VME BSPs. With the use of the provided help documentation, these libraries are easily ported to any 32-bit O/S such as PSOS or Linux.

The latest version of a board specific SSK can be downloaded from our website www.naii.com. Select the software *downloads* section. A Quick-Start Software Manual is also available for download where the SSK contents are detailed, Quick-Start Instructions provided and GUI applications are described therein.

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SPECIFICATIONS

General	For the Mother Board
VME Data transfer:	Data transfers within 200 ns
Interrupts:	One Interrupt capability is implemented. One of seven priority lines can be specified.
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power (Mother board only):	+5 VDC at TBD A, then add power for each individual module.
Temperature, operating:	"C" =0°C to +70°C, "E" =-40°C to +85°C (see part number)
Storage temperature:	-55°C to +105°C
Temperature cycling:	Each board is cycled from -40°C to +85°C for 24 hrs for options “E” or “H” (see P/N)
Size:	6U (9.2") height, 4HP (0.8") width. 233.4 mm x 20.3 mm x 160 mm deep
Weight:	16 oz. (454g) unpopulated. add weight for each module (see module specification) add 2 oz. (57g) for optional reference supply add 2 oz. (57g) for wedge locks

A/D (Module C1)	Ten (10) A/D (1.25 VDC to 10.0 VDC FS) Uni or bipolar
Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or uni-polar channels. Programmable, per channel, as F.S. inputs of: 10.00, 5.00, 2.50, or 1.25 volts where range is ±FS or 0 to FS VDC. The ability to set lower voltages for Full Scale, assures the utilization of the full resolution.
Over-voltage.	No damage up to ±12 V continuous; ±30 V momentary
Open Input sense:	This module will sense and report unconnected Inputs
Input Impedance:	1 MΩ typ.
Accuracy:	0.05 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB’s max. over temperature
Sampling rate:	200 KHz (maximum) per channel
Band Width:	20 KHz
Group delay:	30 microseconds (time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates an optional fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz
Common mode voltage:	Signal voltage plus Common mode equals 10.5 volts
Output Logic:	Bipolar output in two's complement. 7FFF is max. positive, 8000 is max. negative. Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns.
Power:	+5 VDC at 500 ma typical, 750 ma max.
Weight:	1 oz. (28g)

A/D (Module C2) — Ten (10) A/D (40VDC) Uni or bipolar

Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as full scale inputs of: 40.00, 20.00, 10.00, or 5.00 volts where range is ±FS or 0 to FS VDC. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution. This module will not sense open Inputs
Over-voltage protected:	±100 Volts
Input Impedance:	500 kΩ min. (Differential)
Accuracy:	0.1 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB's max. over temperature
Sampling rate:	200 KHz per channel
Bandwidth:	20 KHz per channel
Group delay:	30 microseconds (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter with a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz
Output Logic:	Bipolar output in two's complement. 7FFF is max. positive, 8000 is max. negative. Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	+5 VDC at 500 ma typical, 750 ma max.
Weight:	1 oz. (28g)

A/D (Module C3) — Ten (10) 4-20ma Current Measurement Module

Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input, 0-25ma)
Input scaling:	Ten (10) unipolar channels, 0-25ma full scale. This module will not sense open Inputs
Input voltage:	Not to exceed ±3 volts.
Input Impedance:	100 Ω min.
Accuracy:	0.1 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±8 LSB's max. over temperature
Sampling rate:	200 KHz per channel
Bandwidth:	20 KHz per channel
Group delay:	30 microseconds (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter with a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz
Common mode voltage:	Signal voltage plus Common mode equals 80 volts
Output Logic:	Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	+5 VDC at 500 ma typical, 750 ma max.
Weight:	1 oz. (28g)

A/D (Module C4) — Ten (10) A/D (50VDC) Uni or bipolar

Resolution:	16 bit A/D converters. One per channel
Input format:	Differential (may be used as single ended by grounding one input)
Input scaling:	Ten (10) bipolar or unipolar channels. Programmable, per channel, as full scale inputs of: 50.00, 25.00, 12.50, or 6.25 volts where range is ±FS or 0 to FS VDC. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution. This module will not sense open Inputs
Over-voltage protected:	±100 Volts
Input Impedance:	500 kΩ min. (Differential)
Accuracy:	0.1 % FS over temperature. (no missing codes to 16 bits)
Linearity error:	±1.25 LSB's max. over temperature
Sampling rate:	200 KHz per channel
Bandwidth:	20 KHz per channel
Group delay:	30 microseconds (Time for data sample to propagate to data register)
Programmable filter:	Each channel incorporates a fixed second order anti-aliasing filter and a post filter that has a digitally adjustable break point (programmable from 10 Hz to 10 KHz in 10 Hz steps).
Common mode rejection:	70 dB min. at 60 Hz. Roll off to 50 dB min. at 10 KHz
Common mode voltage:	Signal voltage plus Common mode equals 80 volts
Output Logic:	Bipolar output in two's complement. 7FFF is max. positive, 8000 is max. negative. Unipolar output range from 0 to FFFF full scale
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	+5 VDC at 500 ma typical, 750 ma max.
Weight:	1 oz. (28g)

I/O (Module D7) — Sixteen (16) TTL, Programmable for Input or Output

Input

Input levels:	TTL and CMOS compatible, single ended inputs Each channel incorporates a 100 KΩ pull-down resistor
	$V_{in\ L:}$ 0.8 V = "0"
	$V_{in\ H:}$ 2.0 V = "1"
	$V_{in\ max.:}$ 5.0 V
	I_{IN} = ± 50μA
Read Delay:	1.02 μseconds
De-bounce:	Programmable per bit from 0 to 255 microseconds. LSB= 1 microsecond.

Output

Output levels:	TTL/CMOS, single ended outputs
Drive Capability:	$V_{out\ L:}$ +0.5 V max. sink 32 mA max. $V_{out\ H:}$ 3.8 V min. source -32 mA max.
Output current:	Channel will withstand a current of 50ma for 4 microseconds and will then be turned off.
Rise/Fall time:	10 ns into a 50pf load
Write Delay:	1.02 μseconds
Power:	+5 VDC System Logic Supply, at 40mA per module
Weight:	1 oz. (28g)

I/O (Module D8)	**Eleven (11) Differential Multi-Mode Transceivers**	
Mode of Operation:	422 (Differential)	485 (Differential)
Input		
Receiver Input Levels:	-10V to +10V	-7V to +12V
Receiver Input Resistance:	120Ω	>12kΩ
Receiver Input Sensitivity:	±200mV	±200mV
	(Each channel incorporates a 120 Ω termination resistor that can be programmed on a channel by channel basis)	
Read Delay:	1.02 μseconds	
Filtering	1-128, μseconds programmable	
Output		
Driver Output Voltage:	-0.25V to +6V max.	-0.25V to +6V max.
Driver Output Signal Level (Loaded minimum)	±2V	±1.5V
Driver Output Signal Level (Unloaded maximum)	±6V	±6V
Driver Load Impedance:	100Ω	54Ω
Max. Driver Current in Hi Z State (Power ON):	N/A	±100μA
Max. Driver Current in Hi Z State (Power OFF):	±100μA	±100μA
Write Delay:	1.02 μseconds	
Protection:	Short circuit protected, Thermal shutdown, Built-in current limiting	
Rise/Fall time:	31 ns into a 50pf load	
Power (Per 11 channel module):	+5VDC at 1 Watt quiescent, 1.8Watts fully loaded (54Ω load per channel)	
Weight:	1 oz. (28g)	

Signal (Module E5)	**Four (4) Programmable Frequency Generators**
Output Signal:	Sine, Triangular, or Square Wave, one per channel
Output Frequency:	10 – 130kHz with 1Hz resolution
Output Voltage:	0 – 10Volts peak (7.07Vrms), Programmable, per channel
Accuracy	± 6% FS volts, for frequencies <100Hz
	± 1% FS volts, 100Hz – 20kHz
	± 6% FS volts, for frequencies >20kHz
Load:	600 ohms min.
Regulation:	7% max. No load to full load.
Phase:	0 – 359.912 ±1% with 0.088° resolution, relative to channel 1. Default is 0.
Power:	+5 VDC at 0.6A per module
Weight:	1 oz. (28g)

D/A (Module F1)	**Ten (10) D/A Outputs ±10 VDC , isolated from VME GND.**
Output range:	±10 VDC or 0 to 10 VDC, programmable. For other ranges contact customer service. Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Non-linearity:	0.01% FS over temperature
Gain error:	0.02% over temperature
Output format:	Optically isolated in groups of ten (250 V to VME power)
Settling time:	10 μs typ. (15 μs max)
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	5 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g)

D/A (Module F3)	**Ten (10) D/A Outputs ±5 VDC, isolated from VME GND.**
Output range:	±5 VDC or 0 to 5 VDC, programmable. For other ranges contact customer service. Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Non-linearity:	0.01% FS over temperature
Gain error:	0.02% over temperature
Output format:	Optically isolated in groups of ten (250 V to VME power)
Settling time:	10 μs max
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	5 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g)

D/A (Module F5)	**Four (4) D/A Outputs ±20VDC at 100 mA, isolated from VME GND.**
Output range:	±20 VDC or 0 to 20 VDC, programmable. Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Non-linearity:	0.01% FS over temperature
Gain error:	0.02% over temperature
Output format:	Optically isolated in groups of ten (250 V to VME power)
Settling time:	10 μs max
Load:	100 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. Short circuit protected. When current exceeds 110 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	5 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g)

RTD (Module G4)	**Six (6) four-wire Platinum RTD**
Resolution:	16 bits
RTD Interface:	Interfaces with 100Ω and 500Ω RTDs, or any RTD whose operating resistance is up to 2000Ω under the required operating conditions.
Open Input sense:	This module will sense unconnected Inputs. Only one open wire out of four will set flag
Excitation:	1 milliamp/channel
Accuracy:	0.8Ω for 2kΩ range, over temperature and with a 3.75 Hz bandwidth 0.27Ω for 655Ω range, over temperature and with a 3.75 Hz bandwidth
Grounds:	Each input has a separate return, but all are common and connected to VME ground.
Update rate:	Each channel is updated seven times per second
Output Format:	Resistance
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns.
Power:	+ 12 VDC at 25 ma typical 50 ma max. +5 VDC at 320 ma typical, 500 ma max
Weight:	1 oz. (28g)

D/A (Module J3):	**Ten (10) D/A Outputs ±1.25 VDC, isolated from VME GND.**
Output range:	±1.25 VDC or 0 to +1.25 VDC, programmable. For other ranges contact factory Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Output format:	Optically isolated in groups of ten (250 V to VME power)
Settling time:	10 μs max.
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. 5 KΩ min. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	5 microseconds/channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns.
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max.
Weight:	1 oz. (28g)

D/A (Module J5)	**Ten (10) D/A Outputs ±2.5 VDC, isolated from VME GND.**
Output range:	±2.5 VDC or 0 to +2.5 VDC, programmable. For other ranges contact factory Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Output format:	Optically isolated in groups of ten (250 V to VME power)
Settling time:	10 μs max
Load:	20 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. 5 KΩ min. Short circuit protected. When current exceeds 20 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	5 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g

D/A (Module J8)	**Four (4) D/A Outputs ±20 to ±80 VDC, isolated from VME GND.**
Output range:	±20 to ±80 VDC. Output is set to 0 at reset or Power-on, Programmable in pairs, from ±20V to ±80V.
Returns:	Each D/A return has separate pins that are common within each module. These returns are isolated from VME ground
Resolution:	12 bits/channel
Accuracy:	0.15% FS
Settling time:	10 μs
Load:	10 ma/channel max.(Source or Sink) up to 80VDC. Short circuit protected.
Output impedance:	<1 Ω
Update rate:	20 μs per channel
Output control:	Via software Enable/Disable of DC/DC converter.
Power:	+5 VDC, 250ma max per module
Weight:	1 oz. (28g)

Discrete (Module K6) — SIXTEEN (16) Channels; 0 to 80 volt discrete, (isolated from VME ground), Programmable for Input or Output. Redundant safe.

INPUT CHARACTERISTICS:

Input range:	0 to +80 VDC for level sensing. For contact sensing, Vcc per channel bank, must be between 3 VDC min. and 80 VDC max. There are 4 channels per bank.
Voltage/Contact Sensing:	Software selectable per bit. Input is self-contained and requires no Vcc. However, if Input is used as a current source to detect switch closures, Vcc will be required.
Input Pulse Detection:	A pulse, of 5µs min. width, will be sensed and indicated by the appropriate Hi–Lo or Lo-Hi Transition Interrupt
Input Impedance:	105kΩ (with or without power applied to module)
Switching Threshold:	Four levels are programmable from 0 to 80 VDC with 10-bit resolution (0.98% FS) On, Off. Short to +V, Short to ground.
Accuracy of Set Point:	The greater of 5% signal value or 0.25 volts
ON/OFF Differential	0.25 V minimum recommended
De-bounce:	Programmable per bit from 0 to 0.655 seconds. LSB= 5 microseconds).
Update Rate:	Each channel is updated every 5 microseconds
Over-Voltage Protection:	100 VDC max.
Ground:	Four Ground pins per module (one for each group of 4 channels). All Grounds are common, but are isolated from VME ground.
Protective circuits:	New protective circuits are incorporated that avoid damage should an Input Signal be applied when Vcc is missing.

OUTPUT CHARACTERISTICS:

Output Range:	0 to +80 VDC Output logic is defined by the user provided Vcc voltage to that channel bank. There are four banks with four channels per bank.
Ground	Four Ground pins per module (one for each group of 4 channels). All Grounds are common, but are isolated from VME ground.
Output Current:	0.5 A max. per channel Short circuit protected. **Total current per module not to exceed 8 A.** Channel will withstand a current of 0.75A for 20ms and will then be turned off.
Output Load:	Directly drive inductive loads (relays); Reverse current protection diode is incorporated.
Output impedance:	0.12 ohms
Output Format:	Low-side switched, high-side switched or push-pull. Programmable per bit
Write Delay:	5 µs
Update Rate:	Each channel is updated every 20 microseconds
Over-Voltage Protection:	100 VDC max.
Thermal protection	is provided
Isolation:	Vcc-to-VME Ground: 500 volts Module-to-VME Power: 500 volts I/O Signal: 500 volts, Digital I/O is opto-isolated from VME bus

Redundant applications:	**Two outputs can be connected in parallel (only *one* output set *on*). The output that is turned off will not pull down the signal of the active output.**
Isolation:	Vcc-to-VME Ground: 500 volts Module-to-VME Power: 500 volts I/O Signal: 500 volts, Digital I/O is opto-isolated from VME bus
Power:	+5VDC at 100 mA. For contact sensing add (Vcc x Iset) x4 per bank of 4
Weight:	0.55 oz. (25gms)
Ground	4 Ground pins per module. All Grounds are common, but isolated from VME ground.

LVDT (Module L*) See P/N Four (4) 2, 3 or 4-wire measurements

Resolution:	16-bit
Accuracy:	0.025% FS
Bandwidth:	Default factory setting is 10% of excitation to 100 Hz max. However, BW is field programmable on a per channel basis. User has to program all parameters for each boot up or parameter will bet set to the default value.
Input format:	LVDT or RVDT
Input voltage:	Auto ranging from 2.0 to 28 Vrms.
Excitation voltage:	Not required for computation of output but should be connected to allow card to check for excitation loss.
Input Impedance:	60 kΩ
Frequency:	Specify between 360 Hz to 20 kHz, (See Part Number)
Phase shift:	Automatically compensates for phase shifts between the transducer excitation and Output up to ±60° (3-wire units ignore phase shift)
Wrap around Self Test:	Three powerful test methods are described in the Programming Instructions.
Power:	+ 5 VDC: 2mA
Weight:	1 oz. (28g)

S/D (Module S*) See P/N Four (4) Synchro/Resolver Measurement

This new generation offers additional programmability. Any channel is programmable for either Synchro or Resolver. The Band width will default to a factory set value (generally 10% of reference frequency) but will be field programmable. User has to program all parameters for each boot up or parameter will bet set to the default value.

Resolution:	16 bits (up to 24 bits for two-speed configuration)
Accuracy:	±1 arc-minute for single speed inputs ±1 arc-minute divided by the gear ratio for two-speed inputs
Tracking Rate:	150 RPS (Referred to the Fine input for two-speed configuration)
Bandwidth:	Default set at factory but per channel field programmable.
Input format:	Synchro/Resolver programmable. Default will be Synchro
Input voltage:	See P/N
Input Impedance:	60 kΩ min. at 26V_{L-L}; 260 kΩ min. at 90V_{L-L}
Reference Input:	See P/N.
Reference Zin	100 kΩ min.
Frequency Input:	50 Hz to 20 KHz (See part number)
Angle change alert:	Each channel can be set to a different angle differential. When that differential is exceeded, an interrupt (if enabled) is triggered. Default: “Ch. Disabled”. MSB=180°; Min. differential is 0.05°. Max differential that can be programmed is 179.9°.
Phase shift:	The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°.
Velocity, Digital:	16-bit resolution; Linearity: 0.1%. Scalable to 0.1°/sec resolution.
Wrap around Self Test:	The three different powerful test methods are detailed in the Description section and further described in the Programming Instructions.
Power:	+ 5 VDC: 2mA at 26V_{L-L}; 6mA at 90V_{L-L}
Weight:	1 oz. (28g)

Reference supply, optional

When specifying the reference source that is in addition to the six slots, slot 1 must be populated with either an S/D, or LVDT module or be left empty. If a second reference source (W1) is required, it will use up one of the six slots. (see P/N)

Voltage:	2.0-28Vrms programmable, resolution 0.1Vrms, or 115Vrms Fixed. (See P/N)
Accuracy:	±2%
Frequency:	360Hz to 20kHz ±1% with 1Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	5VA max. @ 40° min. inductive; 178mA RMS @ 2-26VAC or 44mA RMS @ 115VAC Note: Power is reduced linearly as the Reference Voltage.
Power Dissipation:	1A @ 5VA Load (3A peak)
Weight:	2 oz. (28g)

Reference (Module **W1**)	See P/N
Voltage:	2.0-115 Vrms programmable, resolution 0.1Vrms
Accuracy:	±2%
Frequency:	47Hz to 10kHz ±1% with 1Hz resolution.
Regulation:	10% max. No load to full load.
Output power:	2.2 VA max. @ 40° min. inductive; 78mA @ 2-26VAC or 19mA @ 115VAC Note: Power is reduced linearly as the Reference Voltage is reduced.
Power Dissipation:	1A @ 5VA Load (3A peak)
Weight:	2 oz. (28g)

ADDRESS CONFIGURATION

The VME bus interface will respond to A32:D16, A24:D16 and A16:D16 DTB cycles.

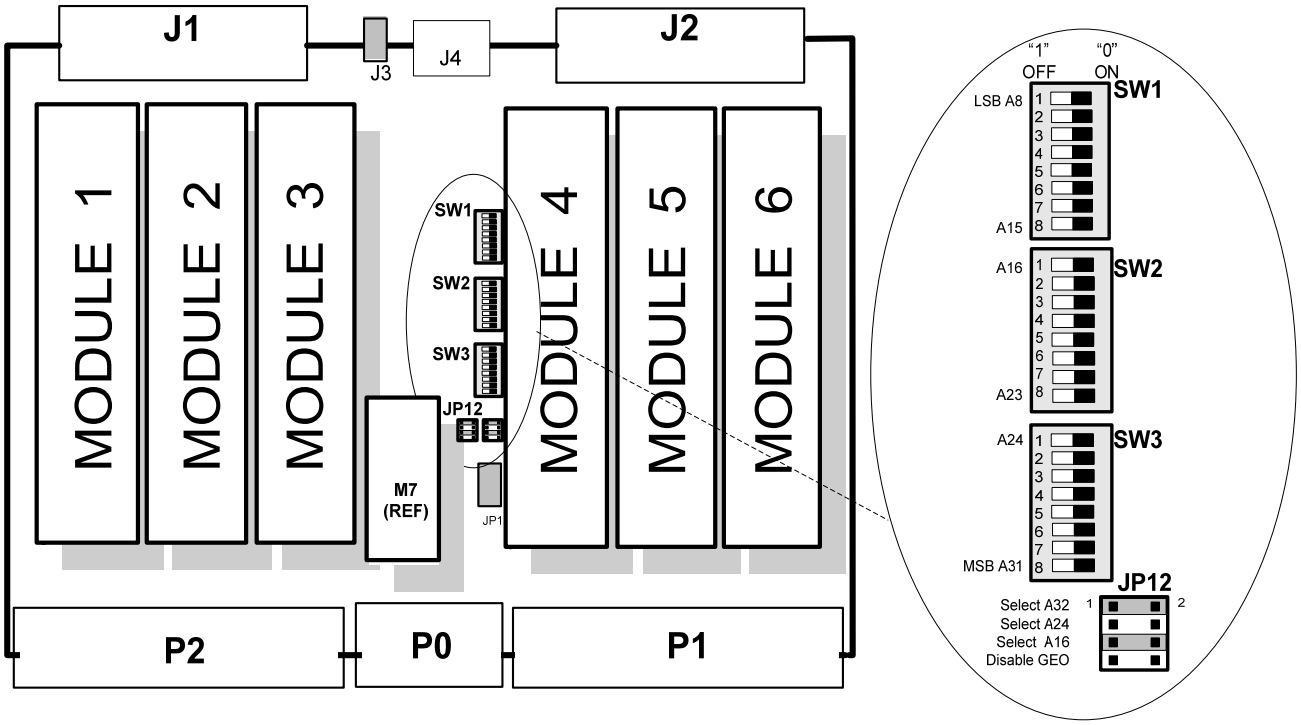
A32 mode:
Unit responds to address modifiers 0A, 0D, 0E and 09. Base address can be set anywhere in the 4 Gigabyte address space on 256 byte boundaries.

A24 mode:
Responds to address modifiers 3A, 3D, 3E and 39. Base address can be set anywhere in the 16 Megabyte address space on 256 byte boundaries.

A16 mode:
Responds to address modifiers 2A, 2D, 2E and 29. Base address can be set anywhere in the 64 K byte address space on 256 byte boundaries.

Geographical Addressing
Enable Geographical Addressing by removing jumper from JP2. Disable Geographical Addressing by adding jumper to JP2. See card layout pictorial below. For detail examples, see 64xxx_VME_Board_Addressing document on our website.

Note: Card requires 2048 byte boundaries. Base addresses for multiple cards in a system must accommodate 2K byte minimum boundaries per card.

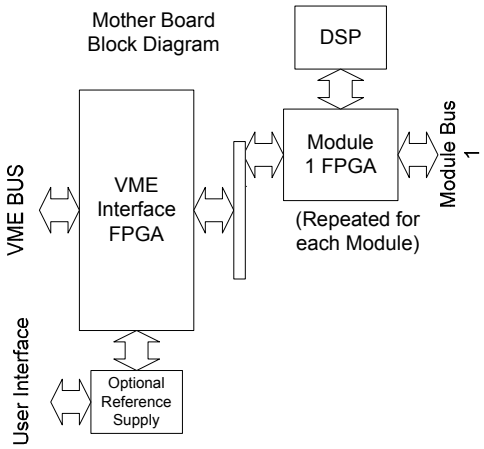


This card will respond to address modifier 2Fh for A24 Address mode, where the 5 Msb's of the A24 address are the 5 bits defined by the slot in VME back plane. The Card can optionally be interrogated at 2Fh to determine resource requirements and available functionally. Using the address modifier 2Fh, the following need to be written to the card:

The base address the card should to respond to
The address modifier (A16, A24, A32)
Then enable the card.

For example : If the card is in slot # 10 the 5 Msb's are 01010 so the address of the CSR registers are :
0101 0 111 1111 1111 xxxx xxxx or 57FFxx h (xx is CSR register offset)
Write to address 57FF63 h, the A31 – A24 base address bits , for example 01h
Write to address 57FF67 h, the A23 – A16 base address bits, for example 02h
Write to address 57FF6B h, the A15 – A8 base address bits, for example 04h
Write to address 57FF6F h, the address modifier you wish to respond to shifted up 2 bits , for example 28h(0A<< 2)
Then Write to address 57FFFBh , 10h to enable the card.
The card will now respond to the base address (010204 in the example) and address modifier (0A in example) programmed. The base address and address modifier can be changed at any time.

PRODUCT CONFIGURATION AND MEMORY MAP



This design provides multiple functions on a single VME card. When ordering, the customer selects an assortment of up to 6 modules to populate this 6-slot "mother board." The memory map follows the order of modules specified in the part number.

To address the register of any module, use the *Base* address to the entire card, add the *Module Offset* depending upon its slot (000, 100, 200,…or 500), and then add the *Register Offset* of interest (see module memory map.) The memory map of each selected module counts from, or is superimposed over its respective module offset. Thus, **Address = Base + Module Offset + Register Offset**.

For example, if a Digital I/O module were selected to populate module 1 and a Discrete I/O module were selected to populate module 4:

Address = Base + Module 1 Offset 010 + Digital I/O register 000 = Base + 010 hex
Address = Base + Module 4 Offset C00 + Discrete I/O register 022 = Base + C22 hex.

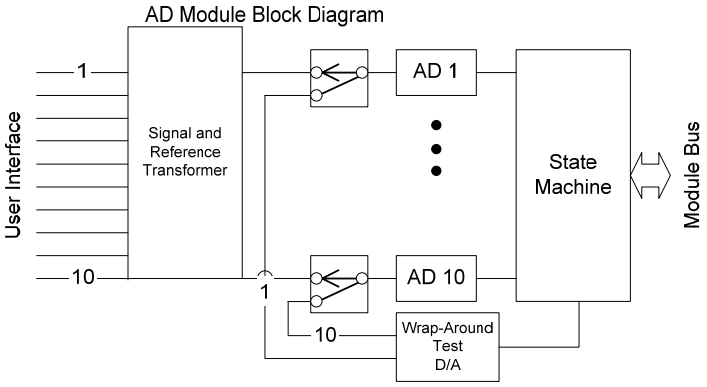
MEMORY MAP

0000	Module 1 Register…	0800	Module 3 Register…	1000	Module 5 Register…
0002		0802		1002	
0004		0804		1004	
0006		0806		1006	
0008	Module 1	0808	Module 3	1008	Module 5
.	Offset 000	.	Offset 800	.	Offset 1000
.		.		.	
.		.		.	
03FC		0BFC		13FC	
03FE		0BFE		13FE	

0400	Module 2 Register…	0C00	Module 4 Register…	1400	Module 6 Register…
0402		0C02		1402	
0404		0C04		1404	
0406		0C06		1406	
0408	Module 2	0C08	Module 4	1408	Module 6
.	Offset 400	.	Offset C00	.	Offset 1400
.		.		.	
.		.		.	
07FC		0FFC		17FC	
07FE		0FFE		17FE	

The memory map of each module type is described hereafter:

A/D (MODULE C)



A/D channels use individual A/D converters with a high (200 kHz) sampling rate per channel. The input range and gain is field programmable for each channel. Each of these differential channels includes a second order anti-aliasing filter and a post filter that has a digitally programmable break point that enables user to field adjust the filtering for each channel. All A/D channels are self-calibrating because each channel, on a rotating basis, is automatically calibrated to eliminate offset and gain errors. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution (does not apply to Current Measurement Module C3 which is fixed unipolar, 0-25mA FS). Open inputs cannot be sensed because scaling input resistor networks are used. All inputs are double buffered for immediate availability. The "Latch" feature permits the user to read all A/D channels at the same time.

The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 0.2% FS. Any failure triggers an Interrupt (if enabled) with the results available in BIT status register. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

In addition, all channels are monitored for open input (except for Current Measurement Module C3 applications).

The (D3) test starts an initiated BIT test that disconnects all A/D's from the I/O and then connects them across an internal stimulus. Each channel will be checked to a test accuracy of 0.2% FS and monitored for open inputs. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from "1" to "0". The test can be stopped at any time and requires no user programming and can be enabled or disabled via the bus.

A (D0) test is used to check the card and VME interface. Write "1" to D0 of *Test enable* register to disconnect all A/D channels from the I/O and connects them across an internal D/A. Test parameters are controlled by the user and are entered in the *D0 Test Voltage* and *DO Test Range* registers. The outputs from the A/D channels are monitored by an internal D/A for proper conversion. External reference voltage is not required

A/D Open Circuit monitoring is disabled during D3 testing.

The 64C2 now includes A/D FIFO Buffering for greater control of the incoming signal (data) for analysis and display. The A/D buffer will accept and/or manipulate the data based on the setting of the base A/D rate. The data can be "stored" in the buffer at the same rate as the Base A/D rate or by a divided multiple as set in the Sample Rate Register. The thresholds of the buffer can be utilized for data flow control.

MODULE MEMORY MAP

000	Data 1	R	014	Range & Polarity[1] 1	R/W	028	Filter Break Freq. 1	R/W	100	CH1 FIFO Buffer Data	R
002	Data 2	R	016	Range & Polarity 2	R/W	02A	Filter Break Freq. 2	R/W	102	CH2 FIFO Buffer Data	R
004	Data 3	R	018	Range & Polarity 3	R/W	02C	Filter Break Freq. 3	R/W	104	CH3 FIFO Buffer Data	R
006	Data 4	R	01A	Range & Polarity 4	R/W	02E	Filter Break Freq. 4	R/W	106	CH4 FIFO Buffer Data	R
008	Data 5	R	01C	Range & Polarity 5	R/W	030	Filter Break Freq. 5	R/W	108	CH5 FIFO Buffer Data	R
00A	Data 6	R	01E	Range & Polarity 6	R/W	032	Filter Break Freq. 6	R/W	10A	CH6 FIFO Buffer Data	R
00C	Data 7	R	020	Range & Polarity 7	R/W	034	Filter Break Freq. 7	R/W	10C	CH7 FIFO Buffer Data	R
00E	Data 8	R	022	Range & Polarity 8	R/W	036	Filter Break Freq. 8	R/W	10E	CH8 FIFO Buffer Data	R
010	Data 9	R	024	Range & Polarity 9	R/W	038	Filter Break Freq. 9	R/W	110	CH9 FIFO Buffer Data	R
012	Data 10	R	026	Range & Polarity 10	R/W	03A	Filter Break Freq. 10	R/W	112	CH10 FIFO Buffer Data	R
120	CH1 FIFO words	R	140	CH1 Hi-Threshold	R/W	160	CH1 Lo-Threshold	R/W	180	CH1 Delay	R/W
122	CH2 FIFO words	R	142	CH2 Hi-Threshold	R/W	162	CH2 Lo-Threshold	R/W	182	CH2 Delay	R/W
124	CH3 FIFO words	R	144	CH3 Hi-Threshold	R/W	164	CH3 Lo-Threshold	R/W	184	CH3 Delay	R/W
126	CH4 FIFO words	R	146	CH4 Hi-Threshold	R/W	166	CH4 Lo-Threshold	R/W	186	CH4 Delay	R/W
128	CH5 FIFO words	R	148	CH5 Hi-Threshold	R/W	168	CH5 Lo-Threshold	R/W	188	CH5 Delay	R/W
12A	CH6 FIFO words	R	14A	CH6 Hi-Threshold	R/W	16A	CH6 Lo-Threshold	R/W	18A	CH6 Delay	R/W
12C	CH7 FIFO words	R	14C	CH7 Hi-Threshold	R/W	16C	CH7 Lo-Threshold	R/W	18C	CH7 Delay	R/W
12E	CH8 FIFO words	R	14E	CH8 Hi-Threshold	R/W	16E	CH8 Lo-Threshold	R/W	18E	CH8 Delay	R/W
130	CH9 FIFO words	R	150	CH9 Hi-Threshold	R/W	170	CH9 Lo-Threshold	R/W	190	CH9 Delay	R/W
132	CH10 FIFO words	R	152	CH10 Hi-Threshold	R/W	172	CH10 Lo-Threshold	R/W	192	CH10 Delay	R/W
1A0	CH1 FIFO size	R/W	1C0	CH1 Sample Rate	R/W	1E0	CH1 Clear FIFO	R/W	200	CH1 Buffer Control	R/W
1A2	CH2 FIFO size	R/W	1C2	CH2 Sample Rate	R/W	1E2	CH2 Clear FIFO	R/W	202	CH2 Buffer Control	R/W
1A4	CH3 FIFO size	R/W	1C4	CH3 Sample Rate	R/W	1E4	CH3 Clear FIFO	R/W	204	CH3 Buffer Control	R/W
1A6	CH4 FIFO size	R/W	1C6	CH4 Sample Rate	R/W	1E6	CH4 Clear FIFO	R/W	206	CH4 Buffer Control	R/W
1A8	CH5 FIFO size	R/W	1C8	CH5 Sample Rate	R/W	1E8	CH5 Clear FIFO	R/W	208	CH5 Buffer Control	R/W
1AA	CH6 FIFO size	R/W	1CA	CH6 Sample Rate	R/W	1EA	CH6 Clear FIFO	R/W	20A	CH6 Buffer Control	R/W
1AC	CH7 FIFO size	R/W	1CC	CH7 Sample Rate	R/W	1EC	CH7 Clear FIFO	R/W	20C	CH7 Buffer Control	R/W
1AE	CH8 FIFO size	R/W	1CE	CH8 Sample Rate	R/W	1EE	CH8 Clear FIFO	R/W	20E	CH8 Buffer Control	R/W
1B0	CH9 FIFO size	R/W	1D0	CH9 Sample Rate	R/W	1F0	CH9 Clear FIFO	R/W	210	CH9 Buffer Control	R/W
1B2	CH10 FIFO size	R/W	1D2	CH10 Sample Rate	R/W	1F2	CH10 Clear FIFO	R/W	212	CH10 Buffer Control	R/W
220	CH1 Trig Control	R/W	240	CH1 FIFO Status	R/W	260	CH1 Interrupt Status	R/W	280	Software Trigger	R/W
222	CH2 Trig Control	R/W	242	CH2 FIFO Status	R/W	262	CH2 Interrupt Status	R/W	282	Clk Rate Adder Input Hi	R/W
224	CH3 Trig Control	R/W	244	CH3 FIFO Status	R/W	264	CH3 Interrupt Status	R/W	284	Clk Rate Adder Input Lo	R/W
226	CH4 Trig Control	R/W	246	CH4 FIFO Status	R/W	266	CH4 Interrupt Status	R/W	288	Rate Mode Control	R/W
228	CH5 Trig Control	R/W	248	CH5 FIFO Status	R/W	268	CH5 Interrupt Status	R/W			
22A	CH6 Trig Control	R/W	24A	CH6 FIFO Status	R/W	26A	CH6 Interrupt Status	R/W	37C	A/D Test Enable	R/W
22C	CH7 Trig Control	R/W	24C	CH7 FIFO Status	R/W	26C	CH7 Interrupt Status	R/W	380	BIT Status Ch.1-10	R
22E	CH8 Trig Control	R/W	24E	CH8 FIFO Status	R/W	26E	CH8 Interrupt Status	R/W	382	Open Status[2] Ch.1-10	R
230	CH9 Trig Control	R/W	250	CH9 FIFO Status	R/W	270	CH9 Interrupt Status	R/W	384	BIT Stat Interrupt Enable Ch.1-10	R/W
232	CH10 Trig Control	R/W	252	CH10 FIFO Status	R/W	272	CH10 Interrupt Status	R/W	386	Open Stat INTR Enable Ch.1-10	R/W
						0F0	A/D Latch		3B4	Module Design Version	R
						0F2	D0 Test Range		3B6	Module Design Revision	R
						0F4	D0 Test Voltage		3B8	Module DSP	R
									3BA	Module FPGA	R
									3BC	Module ID	R

Note: 1. Range & Polarity Register is simply called Range Register in software driver/library.
Range & Polarity does not apply to Current Measurement Module C3
2. Open Status does NOT apply to High Voltage (20V to 80V), or Current Measurement modules.

Data Read

Two's complement format for bipolar mode; 7FFFh=+FS, 8,000h=-FS. For unipolar mode, range is from 0h to FFFFh = FS.

A/D Range & Polarity

Format input for range and polarity. Range is dependent upon Module. Encode range using data bits D0 through D3. Program polarity using data bit D4. Enter per table. Does not apply to Current Measurement Module (C3 is fixed unipolar, 0-25mA FS).

REGISTER	D15	D1	D1	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RANGE & POLARITY	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**

MODULE	C4	C2	C1					
Uni-polar RANGE	0 – 50.0 V	0 – 40.0 V	N/A	**0**	**1**	**0**	**1**	**0**
	0 – 25.0 V	0 – 20.0 V	N/A	**0**	**1**	**0**	**0**	**1**
	0 – 12.5 V	0 – 10.0 V	0 – 10.0 V	**0**	**0**	**0**	**0**	**0**
	0 – 6.25 V	0 – 5.00 V	0 – 5.00 V	**0**	**0**	**0**	**0**	**1**
	N/A	N/A	0 – 2.50 V	**0**	**0**	**0**	**1**	**0**
	N/A	N/A	0 – 1.25 V	**0**	**0**	**0**	**1**	**1**
	N/A	N/A	N/A	**0**	**0**	**1**	**0**	**0**
Bipolar RANGE	±50.0 V	±40.0 V	N/A	**1**	**1**	**0**	**1**	**0**
	±25.0 V	±20.0 V	N/A	**1**	**1**	**0**	**0**	**1**
	±12.5 V	±10.0 V	±10.0 V	**1**	**0**	**0**	**0**	**0**
	±6.25 V	±5.00 V	±5.00 V	**1**	**0**	**0**	**0**	**1**
	N/A	N/A	±2.50 V	**1**	**0**	**0**	**1**	**0**
	N/A	N/A	±1.25 V	**1**	**0**	**0**	**1**	**1**

A/D Filter Break Frequency

The break frequency is the 3 db point of a single pole low pass filter. Enter desired frequency for each channel between 10 Hz to 10 kHz as a 16 bit binary number. Zero disables filter.

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN VERSION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP
Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA
Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID
Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4331h

Read register to determine Module ID in ASCII. For example, find ASCII "C" in upper byte and ASCII "1" in lower byte, for Module "C1," together 4331h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "C"								ASCII "1"								

BIT Status
Check the corresponding bit for a channel's BIT Status. A "0" =Normal; "1" = Non-compliant A/D conversion (outside 0.2% FS accuracy spec). Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status
Check for an open or disconnect to the A/D input. Status of each channel is indicated at its corresponding bit. A "0" =Normal and "1" = Open. An open or disconnect to the input of an A/D channel is detected within 10 seconds and will latch the corresponding bit in the *Open Status* register. Reading any status bit will unlatch the entire register. Open Status is part of background testing and the status register may be checked or polled at any given time. NOTE: Does not apply to Current Measurement Module C3.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status	X	X	X	X	X	X	Ch. 10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable
Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status Interrupt Enable
Set the bit to enable interrupts for the corresponding channel monitored for Open Status. Open Status does NOT apply to high voltage (20V to 80V) or current measurement modules.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Latch All A/Ds

Latch all A/D channels by writing “1” to D1 of Latch register. Write “0” to unlatch all channels.

A/D D0 Test Range

Specify voltage range for A/D module under test. D0 test is performed only on A/D modules. Enter per table.
NOTE: for Current Measurement Module C3, enter up to 2.5V for 25mA FS, unipolar selection only.

REGISTER	D15	D1	D1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A/D D0 TEST RANGE	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**

MODULE	C4	C2	C1					
RANGE	50.0 V	40.0 V		*	**1**	**0**	**1**	**0**
	25.0 V	20.0 V		*	**1**	**0**	**0**	**1**
	12.5 V	10.0 V	10.0 V	*	**0**	**0**	**0**	**0**
	6.25 V	5.00 V	5.00 V	*	**0**	**0**	**0**	**1**
			2.50 V	*	**0**	**0**	**1**	**0**
			1.25 V	*	**0**	**0**	**1**	**1**

∗ **For bipolar/uni-polar selection, program D4 as “0” for unipolar and “1” for bipolar**.

A/D D0 Test Voltage

Specify voltage to be applied by D0 test to A/D module under test. D0 test is performed only on A/D modules. The Test Voltage applied will be a percentage of the Full Scale Set. If using bi-polar mode, write 16 bit 2’s complement word (7FFFh=+FS, 8000h=-FS). If using uni-polar mode, write 16 bit binary word (range: 0 to FFFFh=FS).

Example 1: if using uni-polar mode with 10v range, enter 8000h for 5v test voltage.
Example 2: if using bi-polar mode with 10v range, enter 4000h for 5v test voltage. Enter C000h for –5v.

A/D FIFO Buffer Operational Description

The A/D Buffer is utilized to have a greater control of the incoming signal (data) for analysis and display. The A/D buffer will accept and/or manipulate the data based on the setting of the base A/D rate. The data can be "stored" in the buffer at the same rate as the Base A/D rate or by a divided multiple as set in the Sample Rate Register. The thresholds of the buffer can be utilized for data flow control.

A/D Data:
The available data in the FIFO buffer can be retrieved in the following VME memory addresses one "WORD" (16bits) at a time. The data is presented in two's complement format depending on the range and polarity setting of the individual channel. For bipolar mode; 7FFFh=+FS, 8,000h=-FS. For unipolar mode, range is from 0h to FFFFh = FS.

Addr	r / w	Description	A/D Data(16Bit hex)
100	r	data ch1	Data Range: (0x0000-0xFFFF)
102	r	data ch2	
104	r	data ch3	
106	r	data ch4	
108	r	data ch5	
10A	r	data ch6	
10C	r	data ch7	
10E	r	data ch8	
110	r	data ch9	
112	r	data ch10	

Words in FIFO:
This is a counter that revolves the number of data in WORD (2 byte) stored in the FIFO buffer. Every time when a read operation is made to the A/D Data memory address, its corresponding "Words in FIFO" counter will be decremented by one. The maximum number of words can be stored in the FIFO is 26,213(0x6665).

Addr	r / w	Description	Words in FIFO(16Bit hex)
120	r	Words in ch1	Data Range: (0x0000-0x6665)
122	r	Words in ch2	
124	r	Words in ch3	
126	r	Words in ch4	
128	r	Words in ch5	
12A	r	Words in ch6	
12C	r	Words in ch7	
12E	r	Words in ch8	
130	r	Words in ch9	
132	r	Words in ch10	

Hi-Threshold:

The hi-threshold level is used to set or reset the high limit bit (B2) of the individual channel status register in VME memory location: 0x240 – 0x252. When the "Words in FIFO" counter is greater than the value stored in the hi-threshold register, the high limit bit (B2) of the channel status register will be set. When the "Words in FIFO" counter is less than or equal to the value stored in the hi-threshold, the high limit bit (B2) of the channel status register will be reset.

Set = "logical 1"
Reset = "logical 0"

Addr	r / w	Description	Hi-Threshold(16Bit hex)
140	rw	Hi-Threshold in ch1	Data Range: (0x0000-0x6665)
142	rw	Hi-Threshold in ch2	
144	rw	Hi-Threshold in ch3	
146	rw	Hi-Threshold in ch4	
148	rw	Hi-Threshold in ch5	
14A	rw	Hi-Threshold in ch6	
14C	rw	Hi-Threshold in ch7	
14E	rw	Hi-Threshold in ch8	
150	rw	Hi-Threshold in ch9	
152	rw	Hi-Threshold in ch10	

Low-Threshold:

The low-threshold level is used to set or reset the low limit bit (B1) of the individual channel status register in VME memory location: 0x240 – 0x252. When the "Words in FIFO" counter is greater than or equal to the value stored in the low-threshold, the low limit bit (B1) of the channel status register will be reset. When the "Words in FIFO" counter is less than the value stored in the low-threshold, the low limit bit (B1) of the channel status register will be set.

Set = "logical 1"
Reset = "logical 0"

Addr	r / w	Description	Low-Threshold(16Bit hex)
160	rw	Low-Threshold in ch1	Data Range: (0x0000-0x6665)
162	rw	Low-Threshold in ch2	
164	rw	Low-Threshold in ch3	
166	rw	Low-Threshold in ch4	
168	rw	Low-Threshold in ch5	
16A	rw	Low-Threshold in ch6	
16C	rw	Low-Threshold in ch7	
16E	rw	Low-Threshold in ch8	
170	rw	Low-Threshold in ch9	
172	rw	Low-Threshold in ch10	

Delay:

Set the number of delay samples before the actual FIFO data collection begins. The data collected during the delay period will be discarded.

Addr	r / w	Description	Delay(16Bit hex)
180	rw	Delay in ch1	Data Range: (0x0000-0xFFFF)
182	rw	Delay in ch2	
184	rw	Delay in ch3	
186	rw	Delay in ch4	
188	rw	Delay in ch5	
18A	rw	Delay in ch6	
18C	rw	Delay in ch7	
18E	rw	Delay in ch8	
190	rw	Delay in ch9	
192	rw	Delay in ch10	

Size:

Set the size of the FIFO buffer. The largest size that a FIFO buffer can be is 26,213(0x6665)

Addr	r / w	Description	Size(16Bit hex)
1A0	rw	Size in ch1	Data Range: (0x0000-0x6665)
1A2	rw	Size in ch2	(If size is set to 0, the buffer will be continuously filled
1A4	rw	Size in ch3	
1A6	rw	Size in ch4	
1A8	rw	Size in ch5	
1AA	rw	Size in ch6	
1AC	rw	Size in ch7	
1AE	rw	Size in ch8	
1B0	rw	Size in ch9	
1B2	rw	Size in ch10	

Sample Rate:

The sample rate sets the sampling rate for the FIFO buffer. The number entered in the Sample Rate register will be the divisor of the actual Base A/D sample rate (Clock Rate Control). For example, if the Clock Rate Registers are set to a Base A/D Sample Rate of 44100 (or 44.1 KHz) and the Sample Rate register is set to 2, then every other sample will be stored in the Data Buffer (44.1 Khz / 2 or an "effective" sample rate of 22.05 KHz will reside in the Data Buffer). For full Base A/D clock (sample) rate to be stored in the buffer, the sampling rate would be set to "1".

Addr	r / w	Description	Sample Rate(16Bit hex)
1C0	rw	Rate in ch1	Data Range: (0x0001-0xFFFF)
1C2	rw	Rate in ch2	
1C4	rw	Rate in ch3	
1C6	rw	Rate in ch4	
1C8	rw	Rate in ch5	
1CA	rw	Rate in ch6	
1CC	rw	Rate in ch7	
1CE	rw	Rate in ch8	
1D0	rw	Rate in ch9	
1D2	rw	Rate in ch10	

Clear FIFO:

Whenever the Clear memory is reset for the individual channel, it initializes the "Words in FIFO" to zero. A read to the "A/D Data" register gives aged data. A "write" of 0x0h initiates the clear. All the counters are reset and start again.

Addr	r / w	Description	Clear FIFO(16Bit hex)
1E0	rw	Clear in ch1	Data Range: (0x0000)
1E2	rw	Clear in ch2	
1E4	rw	Clear in ch3	
1E6	rw	Clear in ch4	
1E8	rw	Clear in ch5	
1EA	rw	Clear in ch6	
1EC	rw	Clear in ch7	
1EE	rw	Clear in ch8	
1F0	rw	Clear in ch9	
1F2	rw	Clear in ch10	

Buffer Control:

Different types of data format can be stored in the FIFO buffer and their formats are defined by the Buffer Control Register. The following bit mask defines the type/format of data that will be put into the FIFO buffer.

B0 = Data (16 Bit Hi). 16 bit resolution data for unipolar and bipolar.

B1 = Data (8 Bit Lo). Combine with B0 to form a 24 bit resolution for unipolar and bipolar data.

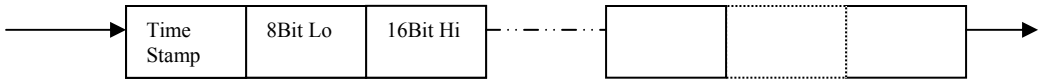
B2 = N/A

B3 = Select Filtered / Un-Filtered Data Mode
(0 = Unfiltered Data, "1" = Filtered Data)

B4 = Time Stamp.
A "free running" integer counter that runs at the "Base Rate" (as set by the Clock Rate Input Control Registers) that counts from 0 to 65535 and wraps around when it overflows.

B5 = Reserved
B6 = Reserved
B7 = Reserved

Note: The data format (B0 – B1) requires one word of storage space from the FIFO buffer. For example, if B0, B1 and B4 are set (0x13) and the Size register is set to 1, a FIFO write will put 3 words of data to the FIFO memory spaces. Since the maximum physical size of FIFO is 26,213 for each channel, the value in the Size and Buffer Control register could cause an overflow to the FIFO buffer. When an overflow condition occurred, any un-stored data will be lost.



FIFO Buffer For Each Write

Addr	r / w	Description	Buffer Ctrl.(16Bit hex)
200	rw	Buf. Ctrl. in ch1	Data Range: b0-b4
202	rw	Buf. Ctrl. in ch2	
204	rw	Buf. Ctrl. in ch3	
206	rw	Buf. Ctrl. in ch4	
208	rw	Buf. Ctrl. in ch5	
20A	rw	Buf. Ctrl. in ch6	
20C	rw	Buf. Ctrl. in ch7	
20E	rw	Buf. Ctrl. in ch8	
210	rw	Buf. Ctrl. in ch9	
212	rw	Buf. Ctrl. in ch10	

Trigger Control:

The FIFO can be started/triggered by different sources (either software control or via external pulse).

B0-B1 = Source Select (choose one only)

0x0 = Ext. Trigger 2
0x1 = Ext. Trigger 1
0x2 = Software Trigger

B3 = Reserved

B4-B7 = Trigger Type (Choose one only)

0x10 = Negative Slope (applies to Ext Triggers)
0x20 = Trigger Pulse Enable (applies to Ext Triggers)
0x40 = Trigger Pulse/Trigger Enable Select (applies to Ext Triggers)
0x80 = Trigger Clear

Addr	r / w	Description	Trigger Ctrl.(16Bit hex)
220	rw	Trigger Ctrl. in ch1	Data Range: b0-b7
222	rw	Trigger Ctrl. in ch2	
224	rw	Trigger Ctrl. in ch3	
226	rw	Trigger Ctrl. in ch4	
228	rw	Trigger Ctrl. in ch5	
22A	rw	Trigger Ctrl. in ch6	
22C	rw	Trigger Ctrl. in ch7	
22E	rw	Trigger Ctrl. in ch8	
230	rw	Trigger Ctrl. in ch9	
232	rw	Trigger Ctrl. in ch10	

FIFO Status:
The FIFO status register indicates the current condition of the FIFO buffer. B0-B4 is used to show the different condition of the buffer.

B0 = Empty. When “Words In FIFO” register is zero, B0 = 1; otherwise =B0 =0.
B1 = Low Limit. When “Words In FIFO” register” < “Low-Threshold”, B1= 1; otherwise B1 =0.
B2 = High Limit. When “Words In FIFO” register” > “Hi-Threshold”, B2=1; otherwise B2 =0.
B3 = FIFO Full. When “Words In FIFO” register” = 26213, B3=1; otherwise B3 =0.
B4 = Sample Done. When “Words In FIFO” register = “Size”, B4=1; otherwise B4 =0.

Addr	r / w	Description	FIFO Status(16Bit hex)
240	r	FIFO Status in ch1	Data Range: b0-b4
242	r	FIFO Status in ch2	
244	r	FIFO Status in ch3	
246	r	FIFO Status in ch4	
248	r	FIFO Status in ch5	
24A	r	FIFO Status in ch6	
24C	r	FIFO Status in ch7	
24E	r	FIFO Status in ch8	
250	r	FIFO Status in ch9	
252	r	FIFO Status in ch10	

Interrupt Enable:

Interrupt(s) may be enabled based on the following;

B0 = Empty. When “Words In FIFO” register is zero, B0 = 1; otherwise =B0 =0.
B1 = Low Limit. When “Words In FIFO” register” < “Low-Threshold”, B1= 1; otherwise B1 =0.
B2 = High Limit. When “Words In FIFO” register” > “Hi-Threshold”, B2=1; otherwise B2 =0.
B3 = FIFO Full. When “Words In FIFO” register” = 26213, B3=1; otherwise B3 =0.
B4 = Sample Done. When “Words In FIFO” register = “Size”, B4=1; otherwise B4 =0.

Note: When/If an interrupt is enable utilizing the low and high limit thresholds, the interrupt will not be “reset” or generate a new interrupt until the opposite threshold has been crossed (hysteresis). For example, if an interrupt enable is set for High Limit Threshold, once set, a new High Limit Threshold interrupt will not be generated until the Low Limit Threshold has been crossed.

Addr	r / w	Description	FIFO Status(16Bit hex)
260	rw	Interrupt Enable CH1	Data Range: b0-b4
262	rw	Interrupt Enable CH2	
264	rw	Interrupt Enable CH3	
266	rw	Interrupt Enable CH4	
268	rw	Interrupt Enable CH5	
26A	rw	Interrupt Enable CH6	
26C	rw	Interrupt Enable CH7	
26E	rw	Interrupt Enable CH8	
270	rw	Interrupt Enable CH9	
272	rw	Interrupt Enable CH10	

Software Trigger:

Software trigger is used to kick start the FIFO buffer and collection of data. In order to use this operation, the “Trigger Ctrl” register must be set up properly. Setting or resetting the “Software Trigger” will start FIFO data collection for ALL channels.

Addr	R / w	Description	Software Trigger(16Bit hex)
280	rw	Software Trigger	Data Range: 0x0-0xFFFF

Clock Rate Input
(Setting the BASE sample rate clock)

Utilize the Clock Rate Input Registers to set the actual or Base Sample Rate of the A/D (LSB of Clock Rate Input LO = 1 Hz). (32-bit word total)

For example, setting a Base Sample Rate of 44100 Hz would be set by initializing the Clock Rate Input HI and LO registers as such:

44100 = AC44(h);
REG 282 = 0000
REG 284 = AC44(h)

Setting a Base Sample Rate at the maximum 200 KHz would be set by initializing the Clock Rate Input HI and LO registers as such:

200000 = 30D40(h)
REG 282 = 0003(h)
REG 284 = 0D40(h)

Clock Rate Input Hi:

Addr	R / w	Description	Software Trigger(16Bit hex)
282	rw	Clk Rate Adder Input Hi	Data Range: 0x0-0xFFFF

Clock Rate Adder Low:

Addr	R / w	Description	Software Trigger(16Bit hex)
284	rw	Clk Rate Adder Input Low	Data Range: 0x0-0xFFFF

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
282	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
CLK Rate Input (HI)	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

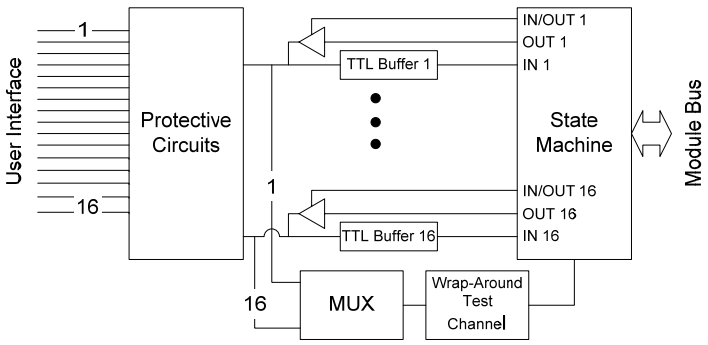
REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
284	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
CLK Rate Input (LO)	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	LSB=1Hz=DATA BIT=D

NOTE: Base Sample Rate Range (combined 32-bit word) 2000 to 200000.

I/O DIGITAL, TTL, (MODULE D7)

Digital (TTL) I/O channels (in banks of 16) are programmable for either Input or Output and include extensive diagnostics. Interrupt can be selected, for each channel, to indicate transition on rising edge, transition on falling edge, or both. De-bounce circuits for each channel offer a selectable time delay to eliminate false signals resulting from contact bounce commonly experienced with mechanical relays and switches. Each TTL channel has an internal 110KΩ pull-down resistor. All inputs are continually scanned and the data is double buffered for immediate availability.

TTL Module Block Diagram



The (D2) test initiates **automatic** background BIT testing which tests and validates channel processing (data read or write logic), tests for circuit over-current conditions and provides status for threshold signal transitioning. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus.

MODULE MEMORY MAP

000	Write Output,	Ch.1-16 R/W	070	Debounce time	Ch.11 R/W	0D0	Status Fault	Ch.01-16	R
002	Read I/O,	Ch.1-16 R/W	07A	Debounce time	Ch.12 R/W	0D4	Status Over-Current	Ch.01-16	R
00C	Debounce time	Ch.1 R/W	084	Debounce time	Ch.13 R/W	0DC	Status Lo-Hi Transition	Ch.01-16	R
016	Debounce time	Ch.2 R/W	08E	Debounce time	Ch.14 R/W	0DE	Status Hi-Lo Transition	Ch.01-16	R
020	Debounce time	Ch.3 R/W	098	Debounce time	Ch.15 R/W	0E8	Interrupt Fault Enable	Ch.01-16	R/W
02A	Debounce time	Ch.4 R/W	0A2	Debounce time	Ch.16 R/W	0EC	Interrupt Over-Current Enable	Ch.01-16	R/W
034	Debounce time	Ch.5 R/W	0A4	Input/Output Format	Ch.01-8 R/W	0F4	Interrupt Lo-Hi Transition Enable	Ch.01-16	R/W
03E	Debounce time	Ch.6 R/W	0A6	Input/Output Format	Ch.09-16 R/W	0F6	Interrupt Hi-Lo Transition Enable	Ch.01-16	R/W
048	Debounce time	Ch.7 R/W	0BC	Reset Over-Current	Ch.1-16 R/W				
052	Debounce time	Ch.8 R/W				3B4	Module Design Version		R
05C	Debounce time	Ch.9 R/W				3B6	Module Design Revision		R
066	Debounce time	Ch.10 R/W				3B8	Module DSP		R
						3BA	Module FPGA		R
						3BC	Module ID		R

Write Output

When a channel is configured for Output, write logic level High (“1”) or Low (“0”) to associated channel bit, in 16 bit binary word. Each bit corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Read I/O

Independent of channel configuration (Input or Output), read logic state High (“1”) or Low (“0”) as defined by channel threshold values. Each bit of 16-bit binary word corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

De-bounce time

Enter required de-bounce time into appropriate channel registers. Enter time in 1.28μs increments up to 326.40 μsec. LSB= 1.28 μs (defaulted). Value is 8 bits (MSBs=don't care). Once a signal level is a logic voltage level period longer than the De-bounce time (Logic High > 2.0 v, and Logic Low < 0.6 v), a logic transition is validated. Signal pulse widths less than De-bounce time are filtered or ignored. Once valid, the interrupt transition register channel flag is set and the output logic changes state. Enter a value of 0 to disable De-bounce filtering. De-bounce defaults to 00h upon reset.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
									163.84	81.92	40.96	20.48	10.24	5.12	2.56	1.28	value in mSec (LSB=1.28μS)
DE-BOUNCE TIME	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input/Output Format

Configure channels in groups of 8. Write integer 0 for input, 3 for output: Default is configured for Input.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INPUT/OUTPUT CH 01-08	Ch.08		Ch.07		Ch.06		Ch.05		Ch.04		Ch.03		Ch.02		Ch.01		Channel
INPUT/OUTPUT CH 09-16	Ch.16		Ch.15		Ch.14		Ch.13		Ch.12		Ch.11		Ch.10		Ch.09		Channel
INPUT/OUTPUT	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT

Integer	D_H	D_L	
0	**0**	**0**	Input
3	**1**	**1**	Output

Reset Over-Current

Write integer "1" to reset all sixteen channels (per module). Used to reset disabled channel(s) following an over-current condition. When reset process is complete, processor will write a "0" back to the *Reset Over-Current* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESET OVER-CURRENT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	D=DATA BIT

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN VERSION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP

Type: binary word
Range: 0 to 65535

Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4431h

Read register to determine Module ID in ASCII. For example, find ASCII “D” in upper byte and ASCII “1” in lower byte for Module “D1,” together 4431h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “D”								ASCII “1”								

Automatic background BIT testing

BIT is always enabled and continually checks that each channel is functional. This capability is accomplished by an additional test comparator that is incorporated into each 16 channel module. The test comparator is sequentially connected across each channel and is compared against the operational channel. Depending upon configuration, the Input data read or Output logic write of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. Low to High and High to Low logic transitions are indicated. Additional testing of output logic indicates Over-current condition when output logic is invalid for a period greater than 80µs.

Status indications

Fault – processing (data read or write logic) is inconsistent with redundant test circuit.
Status is indicated within 15 seconds. A fault is latched until read. (Testing takes approx. 1 second per channel)

Lo-Hi Transition – If a Lo to High transition is sensed, status is indicated (bit is set) within 40µs.
Hi-Low Transition – If a High to Low transition is sensed, status is indicated (bit is set) within 40µs.

Over-current – If over-current or overload condition is sensed, status is indicated (bit is set) within 80µs. Output is however, immediately disabled at time of over-current condition.

When status is "indicated," or bit is "set," bit value is logic "1." Reading will reset (or unlatch) Status Register.

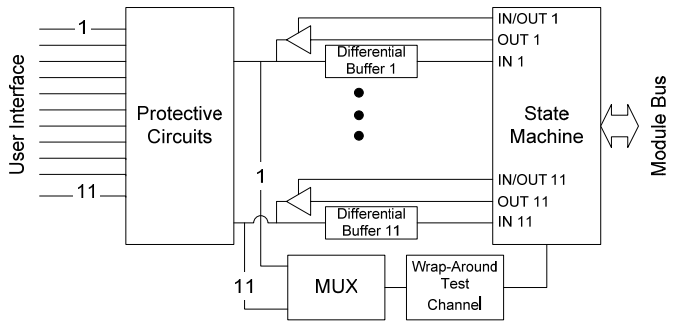
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

I/O DIGITAL DIFFERENTIAL MULTI-MODE TRANSCEIVERS (MODULE D8)

Differential RS422/RS485 I/O channels (in banks of 11) are programmable for either Input or Output and include extensive diagnostics. Each Differential input channel has a selectable internal resistor (120Ω or >12kΩ) across its inputs (RS422). Interrupt can be selected, for each channel, to indicate transition on rising edge, transition on falling edge, or both. De-bounce circuits for each channel offer a selectable time delay to eliminate false signals resulting from contact bounce commonly experienced with mechanical relays and switches. All inputs are continually scanned and the data is double buffered for immediate availability.

The (D2) test initiates **automatic** background BIT testing which tests and validates channel processing (data read or write logic), tests for circuit over-current conditions and fault status. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus.

Differential Module Block Diagram



MODULE MEMORY MAP

000	Write Output,	Ch.1-11 R/W	05C	De-bounce time	Ch.9 R/W	0E8	Interrupt Fault Enable	Ch.01-11 R/W
002	Read I/O,	Ch.1-11 R/W	066	De-bounce time	Ch.10 R/W	0EC	Interrupt Over-Current Enable	Ch.01-11 R/W
00C	De-bounce time	Ch.1 R/W	070	De-bounce time	Ch.11 R/W	0F4	Interrupt Lo-Hi Transition Enable	Ch.01-11 R/W
016	De-bounce time	Ch.2 R/W	0A2	Input Termination	Ch 01-11 R/W	0F6	Interrupt Hi-Lo Transition Enable	Ch.01-11 R/W
020	De-bounce time	Ch.3 R/W	0A4	Input/Output Format	Ch.1-8 R/W	3B4	Module Design Version	R
02A	De-bounce time	Ch.4 R/W	0A6	Input/Output Format	Ch.9-11 R/W	3B6	Module Design Revision	R
034	De-bounce time	Ch.5 R/W	0D0	Status Fault	Ch.01-11 R	3B8	Module DSP	R
03E	De-bounce time	Ch.6 R/W	0D4	Status Over-Current	Ch.01-11 R	3BA	Module FPGA	R
048	De-bounce time	Ch.7 R/W	0DC	Status Lo-Hi Transition	Ch.01-11 R	3BC	Module ID	R
052	De-bounce time	Ch.8 R/W	0DE	Status Hi-Lo Transition	Ch.01-11 R			

Write Output

When a channel is configured for Output, write logic level High (“1”) or Low (“0”) to associated channel bit, in 16 bit binary word. Each bit corresponds to one of 11 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
						11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Read I/O

Independent of channel configuration (Input or Output), read logic state High (“1”) or Low (“0”). Each bit of 16-bit binary word corresponds to one of 11 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
						11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

De-bounce time

Enter required de-bounce time into appropriate channel registers. Enter time in 1.28μs increments, up to 326.40 μsec. LSB= 1.28 μs. Value is 8 bits (MSBs=don't care). Once a signal level is a logic voltage level period longer than the De-bounce time (Logic High > 2.0 v, and Logic Low < 0.6 v), a logic transition is validated. Signal pulse widths less than De-bounce time are filtered or ignored. Once valid, the interrupt transition register channel flag is set and the output logic changes state. Enter a value of 0 to disable De-bounce filtering. De-bounce defaults to 00h upon reset.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
									163.84	81.92	40.96	20.48	10.24	5.12	2.56	1.28	value in mSec (LSB=1.28μS)
DE-BOUNCE TIME	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input Termination Control

Each differential input pair can be programmed to have an input termination of 120 Ω or >96 K Ω. Write logic'1' to select 120 Ω for each individual channel. Default is >96 K Ω.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
						11	10	9	8	7	6	5	4	3	2	1	Channel
INPUT TERMINATION	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input/Output Format

Write integer 0 for input, 3 for output: Default is configured for Input.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INPUT/OUTPUT CH 01-08	Ch.08		Ch.07		Ch.06		Ch.05		Ch.04		Ch.03		Ch.02		Ch.01		Channel
INPUT/OUTPUT CH 09-11											Ch.11		Ch.10		Ch.09		Channel
INPUT/OUTPUT	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT

Integer	D_H	D_L	
0	**0**	**0**	Input
3	**1**	**1**	Output

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP

Type: binary word
Range: 0 to 65535

Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4332h

Read register to determine Module ID in ASCII. For example, find ASCII “D” in upper byte and ASCII “2” in lower byte for Module “D2,” together 4432h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “D”								ASCII “2”								

Automatic background BIT testing

BIT is always enabled and continually checks that each channel is functional. This capability is accomplished by an additional test comparator that is incorporated into each 11 channel module. The test comparator is sequentially connected across each channel and is compared against the operational channel. Depending upon configuration, the Input data read or Output logic write of the operational channel and test comparator must agree or a fault is indicated with the results available in the associated status register. Low to High and High to Low logic transitions are indicated. Additional testing of output logic indicates Over-current condition when output logic is invalid for a period greater than 80µs.

Status indications

Fault – processing (data read or write logic) is inconsistent with redundant test circuit.
Status is indicated within 15 seconds. A fault is latched until read. (Testing takes approx. 1 second per channel)

Lo-Hi Transition – If a Lo to High transition is sensed, status is indicated within 40µs.
Hi-Low Transition – If a High to Low transition is sensed, status is indicated within 40µs.

Over-current – If over-current or overload condition is sensed, status is indicated (bit is set) within 80µs. Output is however, immediately disabled at time of over-current condition. Over-current is re-checked every 6ms. If applicable output is re-enabled and channel is reset.

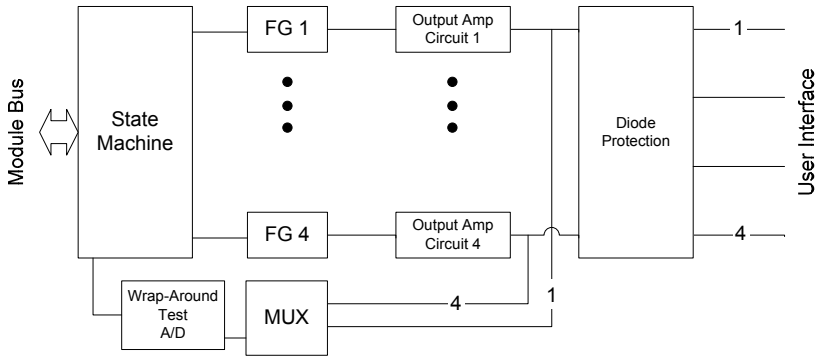
A ”0” indicates Passing and “1” Failing status. Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	X	X	X	X	X	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

SIGNAL GENERATOR (MODULE E5)

Signal Generator modules generate one of a selection of waveforms, sine, triangular, or square wave, per channel, programmable in frequency and amplitude. Use of an individual A/D self test channel, on a rotating basis, verifies that the channel is operating properly in frequency, amplitude, and DC offset. See wrap-around test registers for BIT data

Signal Module Block Diagram



Operating at all times is a background Built-In-Test (BIT), where each channel is checked to a test accuracy of 2% FS. Any failure triggers an Interrupt (if enabled) with the results available in status registers. BIT is intended for use with steady state signals; any change in channel configuration (amplitude, frequency, etc) requires up to 12 seconds before wrap data reflects that change. Multiple changes in channel configuration in less than 12 seconds may trigger false BIT failures. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card.

MODULE MEMORY MAP

000	Ch.1 Frequency High	R/W	020	Ch.3 DC Offset	R/W	050	Ch.3 Wrap-around Frequency High	R
002	Ch.1 Frequency Low	R/W	022	Ch.3 Mode	R/W	052	Ch.3 Wrap-around Frequency Low	R
004	Not used		024	Ch.4 Freq Hi	R/W	054	Ch.3 Wrap-around Amplitude	R
006	Ch.1 Amplitude	R/W	026	Ch.4 Freq Lo	R/W	056	Ch.3 Wrap-around DC Offset	R
008	Ch.1 DC Offset	R/W	028	Ch.4 Phase	R/W	058	Ch.4 Wrap-around Frequency High	R
00A	Ch.1 Mode	R/W	02A	Ch.4 Amplitude	R/W	05A	Ch.4 Wrap-around Frequency Low	R
00C	Ch.2 Freq Hi	R/W	02C	Ch.4 DC Offset	R/W	05C	Ch.4 Wrap-around Amplitude	R
00E	Ch.2 Freq Lo	R/W	02E	Ch.4 Mode	R/W	05E	Ch.4 Wrap-around DC Offset	R
010	Ch.2 Phase	R/W	040	Ch.1 Wrap-around Frequency High	R	0D0	BIT Status Ch.1-4	R
012	Ch.2 Amplitude	R/W	042	Ch.1 Wrap-around Frequency Low	R	0E8	BIT Stat Interrupt Enable Ch.1-4	R/W
014	Ch.2 DC Offset	R/W	044	Ch.1 Wrap-around Amplitude	R	3B4	Module Design Version	
016	Ch.2 Mode	R/W	046	Ch.1 Wrap-around DC Offset	R	3B6	Module Design Revision	R
018	Ch.3 Freq Hi	R/W	048	Ch.2 Wrap-around Frequency High	R	3B8	Module DSP	R
01A	Ch.3 Freq Lo	R/W	04A	Ch.2 Wrap-around Frequency Low	R	3BA	Module FPGA	R
01C	Ch.3 Phase	R/W	04C	Ch.2 Wrap-around Amplitude	R	3BC	Module ID	R
01E	Ch.3 Amplitude	R/W	04E	Ch.2 Wrap-around DC Offset	R			

Frequency

Type: 32 bit unsigned integer
Range: 0 – 130,000 (from 1 to 9 Hz, amplitude is functional, but not to accuracy specification)
Read/Write: R/W
Initialized Value: 1000

Frequency High and *Frequency Low* registers combined to determine desired frequency in 1 Hz resolution. LSB is 1 Hz. Frequency is updated on write to Low register. Out-of-range data will be changed to the maximum allowable value. When phase locked, phase is reset when channel 1frequency is changed. If phase is NOT locked, phase remains unchanged when frequency is changed.

FREQUENCY HIGH REGISTER																FREQUENCY LOW REGISTER															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Phase

Type: 16-bit signed integer
Range: ±180 degrees
Read/Write: R/W
Initialized Value: 0

Enter the desired phase offset, relative to channel 1. LSB is approximately 0.088°. When phase locked, phase is reset when channel 1frequency is changed. If phase is NOT locked, phase remains unchanged when frequency is changed. Enter as per formula,

Phase = Register Value / 32768 x 180 Degrees.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PHASE	S	D	D	D	D	D	D	D	D	D	D	D	X	X	X	X	S=SIGN BIT, D=DATA BIT

Amplitude

Type: 16 bit unsigned integer
Range: 0 to 65535 (0 to 10 volts peak E1 ; 0 to 15 volts peak E2)
Read/Write: R/W
Initialized Value: 0

Value determines peak amplitude of selected waveform. Amplitude in combination with the programmed DC Offset cannot be greater that the maximum or full scale output of that module. For module E1, resolution is 10/65536 or approximately 0.15 millivolts. For module E2 resolution is 15/65536 or approximately 0.22 millivolts. From 1 to 9 Hz, amplitude is not accurate. Enter as per formula,

Peak-to-Peak Voltage = 10*Value/65535 Volts Peak, for module E1, (≤ 10 – magnitude of DC Offet).

Peak-to-Peak Voltage = 15*Value/65535 Volts Peak, for module E2, (≤ 15 – magnitude of DC Offet).

Where Volts Peak is half Peak-to-Peak Voltage. Out-of-range data will be changed to the maximum allowable value. From 1 to 9 Hz, amplitude is functional, but not to accuracy specification.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

DC Offset

Type: 16 bit signed integer
Range: -32767 to +32767 (±10 volts E1 ; ±15 volts E2)
Read/Write: R/W
Initialized Value: 0

Value determines DC offset of selected waveform, in 0.30 millivolt resolution.
Enter as per formula,

DC Offset Voltage = 10*Value/32768 Volts DC, for Module E1

DC Offset Voltage = 15*Value/32768 Volts DC, for Module E2

Out-of-range data will be changed to the maximum allowable value.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Mode

Type: binary word
Range: 0, 1, or 2
Read/Write: R/W
Initialized Value: 0 (Sine Wave)

This register is used to select desired waveform using bits D0 and D1. Use bit D2 to enable phase lock function. L=1 to enable, L=0 to disable. When phase lock is enabled, channel 2, 3, and 4 are phase locked to the master signal channel 1. When phased locked, the signal of channels 2, 3 and 4 will be identical to channel 1 in *frequency* and *type* (sine, triangular or square). When phase locked, phase is reset when frequency is changed.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODE and LOCK	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**0**	**0**	SINE WAVE
	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**0**	**1**	TRIANGULAR WAVE
	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**1**	**0**	SQUARE WAVE
	X	X	X	X	X	X	X	X	X	X	X	X	X	**L**	**1**	**1**	SINE WAVE (same as 00)

Wrap-around Frequency

Type: 32 bit unsigned integer
Range: 0 – 130,000 (from 1 to 9 Hz, amplitude is functional, but not to accuracy specification)
Read/Write: R
Initialized Value: N/A

Read *Wrap-around Frequency High* and *Frequency Low* registers combined to determine desired frequency in 1 Hz resolution. LSB is 1 Hz.

FREQUENCY HIGH REGISTER																	FREQUENCY LOW REGISTER															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

Wrap-around Amplitude

Type: 16 bit unsigned integer
Range: 0 to 65535 (0 to 10 volts peak E1 ; 0 to 15 volts peak E2)
Read/Write: R
Initialized Value: N/A

Read *Wrap-around Amplitude* for D2 BIT test value to verify peak amplitude of selected waveform. For module E1, resolution is 10/65536 or approximately 0.15 millivolts. For module E2 resolution is 15/65536 or approximately 0.22 millivolts. From 1 to 9 Hz, amplitude is not accurate. Decode value as per formula,

Peak-to-Peak Voltage = 10*Value/65535 Volts Peak, for module E1

Peak-to-Peak Voltage = 15*Value/65535 Volts Peak, for module E2

where Volts Peak is half Peak-to-Peak Voltage.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Wrap-around DC Offset

Type: 16 bit signed integer
Range: -32767 to +32767 (±10 volts E1 ; ±15 volts E2)
Read/Write: R
Initialized Value: N/A

Read *Wrap-around DC Offset* for D2 BIT test value to verify DC offset of selected waveform, in 0.30 millivolt resolution. Decode value as per formula,

DC Offset Voltage = 10*Value/32768 Volts DC, for Module E1

DC Offset Voltage = 15*Value/32768 Volts DC, for Module E2

Out-of-range data will be changed to the maximum allowable value.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
AMPLITUDE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII “1” in upper byte and ASCII space in lower byte for Module Design Version “1 ” is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN VERSION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “1”								ASCII “ ”								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII “B” in upper byte and ASCII space in lower byte for Module Design Revision “B ” is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “B”								ASCII “ ”								

Module DSP

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4531h

Read register to determine Module ID in ASCII. For example, find ASCII "E" in upper byte and ASCII "1" in lower byte, for Module "E1," together 4531h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "E"								ASCII "1"								

BIT Status

Type: binary word
Range: 0 to 15
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Built-In-Test (BIT) Status. Channel Status Data bit (Chn, where n is 1, 2, 3 or 4) is fail, high true, and indicates that the channel is not operating spec compliant. Passing BIT status indicates that channel Frequency, Amplitude and DC Offset is as programmed. Status is latched. Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time. BIT is operating at all times and cannot be enabled or disabled using the General use *Test Enable* register.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

BIT Status Interrupt Enable

Type: binary word
Range: 0 to 15
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 0 to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS INTR ENA	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

D/A (MODULES F & J)

Ten (10) D/A channels are provided per module and includes extensive diagnostics. Overloaded outputs will be detected, with the results displayed in a status word. This module incorporates major diagnostic capabilities that offer substantial improvements to system reliability because user is alerted to malfunctions within 5 seconds. Two different tests, one off-line (D2) and one on-line (D3) can be selected:

The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 0.2% FS and monitored for shorted output. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

The (D3) test uses an internal A/D that measures all D/A channels while they remain connected to the I/O. Each channel will be checked to a test accuracy of 0.2% FS. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from "1" to "0". The test can be stopped at any time. This test requires no user programming and can be enabled or disabled via the bus. **CAUTION:** D/A Outputs are active during this test. Check connected loads for interaction.

D/A Over Current (short circuit) monitoring is disabled during D3 testing.

The 64C2 now includes D/A FIFO Buffering for greater control of the output voltage / signal (data). When the Buffer is enabled and triggered, the D/A buffer will accept / store / output the voltage for applications requiring simulation of waveform generation. The data can be "outputted" from the buffer at a maximum D/A Buffer base rate of 390.625 KHz or divided by an integer set in the Sample Rate Register. The thresholds of the buffer can be utilized for data flow control.

D/A MODULE MEMORY MAP

000	Data 1	R/W	028	Filter Break Freq 1	R	050	Trigger 1	R/W	100	CH1 FIFO Buffer Data	W
002	Data 2	R/W	02A	Filter Break Freq 2	R	052	Trigger 2	R/W	102	CH2 FIFO Buffer Data	W
004	Data 3	R/W	02C	Filter Break Freq 3	R	054	Trigger 3	R/W	104	CH3 FIFO Buffer Data	W
006	Data 4	R/W	02E	Filter Break Freq 4	R	056	Trigger 4	R/W	106	CH4 FIFO Buffer Data	W
008	Data 5	R/W	030	Filter Break Freq 5	R	058	Trigger 5	R/W	108	CH5 FIFO Buffer Data	W
00A	Data 6	R/W	032	Filter Break Freq 6	R	05A	Trigger 6	R/W	10A	CH6 FIFO Buffer Data	W
00C	Data 7	R/W	034	Filter Break Freq 7	R	05C	Trigger 7	R/W	10C	CH7 FIFO Buffer Data	W
00E	Data 8	R/W	036	Filter Break Freq 8	R	05E	Trigger 8	R/W	10E	CH8 FIFO Buffer Data	W
010	Data 9	R/W	038	Filter Break Freq 9	R	060	Trigger 9	R/W	110	CH9 FIFO Buffer Data	W
012	Data 10	R/W	03A	Filter Break Freq 10	R	062	Trigger 10	R/W	112	CH10 FIFO Buffer Data	W
014	Polarity 1	R/W	03C	Current Reading 1	R	068	D/A Reset to zero	R/W			
016	Polarity 2	R/W	03E	Current Reading 2	R	06A	D/A Retry Overload	R/W			
018	Polarity 3	R/W	040	Current Reading 3	R	06C	D/A Reset Overload	R/W			
01A	Polarity 4	R/W	042	Current Reading 4	R	06E	D/A Override	R/W			
01C	Polarity 5	R/W	044	Current Reading 5	R						
01E	Polarity 6	R/W	046	Current Reading 6	R	0F0	A/D Latch				
020	Polarity 7	R/W	048	Current Reading 7	R	0F2	D0 Test Range				
022	Polarity 8	R/W	04A	Current Reading 8	R	0F4	D0 Test Voltage				
024	Polarity 9	R/W	04C	Current Reading 9	R						
026	Polarity 10	R/W	04E	Current Reading 10	R						
120	CH1 FIFO words	R	140	CH1 Hi-Threshold	R/W	160	CH1 Lo-Threshold	R/W	180	CH1 Delay	R/W
122	CH2 FIFO words	R	142	CH2 Hi-Threshold	R/W	162	CH2 Lo-Threshold	R/W	182	CH2 Delay	R/W
124	CH3 FIFO words	R	144	CH3 Hi-Threshold	R/W	164	CH3 Lo-Threshold	R/W	184	CH3 Delay	R/W
126	CH4 FIFO words	R	146	CH4 Hi-Threshold	R/W	166	CH4 Lo-Threshold	R/W	186	CH4 Delay	R/W
128	CH5 FIFO words	R	148	CH5 Hi-Threshold	R/W	168	CH5 Lo-Threshold	R/W	188	CH5 Delay	R/W
12A	CH6 FIFO words	R	14A	CH6 Hi-Threshold	R/W	16A	CH6 Lo-Threshold	R/W	18A	CH6 Delay	R/W
12C	CH7 FIFO words	R	14C	CH7 Hi-Threshold	R/W	16C	CH7 Lo-Threshold	R/W	18C	CH7 Delay	R/W
12E	CH8 FIFO words	R	14E	CH8 Hi-Threshold	R/W	16E	CH8 Lo-Threshold	R/W	18E	CH8 Delay	R/W
130	CH9 FIFO words	R	150	CH9 Hi-Threshold	R/W	170	CH9 Lo-Threshold	R/W	190	CH9 Delay	R/W
132	CH10 FIFO words	R	152	CH10 Hi-Threshold	R/W	172	CH10 Lo-Threshold	R/W	192	CH10 Delay	R/W
1A0	CH1 FIFO size	R/W	1C0	CH1 Sample Rate	R/W	1E0	CH1 Clear FIFO	R/W	200	CH1 Buffer Control	R/W
1A2	CH2 FIFO size	R/W	1C2	CH2 Sample Rate	R/W	1E2	CH2 Clear FIFO	R/W	202	CH2 Buffer Control	R/W
1A4	CH3 FIFO size	R/W	1C4	CH3 Sample Rate	R/W	1E4	CH3 Clear FIFO	R/W	204	CH3 Buffer Control	R/W
1A6	CH4 FIFO size	R/W	1C6	CH4 Sample Rate	R/W	1E6	CH4 Clear FIFO	R/W	206	CH4 Buffer Control	R/W
1A8	CH5 FIFO size	R/W	1C8	CH5 Sample Rate	R/W	1E8	CH5 Clear FIFO	R/W	208	CH5 Buffer Control	R/W
1AA	CH6 FIFO size	R/W	1CA	CH6 Sample Rate	R/W	1EA	CH6 Clear FIFO	R/W	20A	CH6 Buffer Control	R/W
1AC	CH7 FIFO size	R/W	1CC	CH7 Sample Rate	R/W	1EC	CH7 Clear FIFO	R/W	20C	CH7 Buffer Control	R/W
1AE	CH8 FIFO size	R/W	1CE	CH8 Sample Rate	R/W	1EE	CH8 Clear FIFO	R/W	20E	CH8 Buffer Control	R/W
1B0	CH9 FIFO size	R/W	1D0	CH9 Sample Rate	R/W	1F0	CH9 Clear FIFO	R/W	210	CH9 Buffer Control	R/W
1B2	CH10 FIFO size	R/W	1D2	CH10 Sample Rate	R/W	1F2	CH10 Clear FIFO	R/W	212	CH10 Buffer Control	R/W
220	CH1 Trig Control	R/W	240	CH1 FIFO Status	R	260	CH1 Interrupt Enable	R/W	280	Software Trigger	R/W
222	CH2 Trig Control	R/W	242	CH2 FIFO Status	R	262	CH2 Interrupt Enable	R/W			
224	CH3 Trig Control	R/W	244	CH3 FIFO Status	R	264	CH3 Interrupt Enable	R/W	288	Rate Mode Control	R/W
226	CH4 Trig Control	R/W	246	CH4 FIFO Status	R	266	CH4 Interrupt Enable	R/W			
228	CH5 Trig Control	R/W	248	CH5 FIFO Status	R	268	CH5 Interrupt Enable	R/W			
22A	CH6 Trig Control	R/W	24A	CH6 FIFO Status	R	26A	CH6 Interrupt Enable	R/W			
22C	CH7 Trig Control	R/W	24C	CH7 FIFO Status	R	26C	CH7 Interrupt Enable	R/W			
22E	CH8 Trig Control	R/W	24E	CH8 FIFO Status	R	26E	CH8 Interrupt Enable	R/W			
230	CH9 Trig Control	R/W	250	CH9 FIFO Status	R	270	CH9 Interrupt Enable	R/W			
232	CH10 Trig Control	R/W	252	CH10 FIFO Status	R	272	CH10 Interrupt Enable	R/W			
37C	Test Enable	R/W	3B4	Module Design Version	R	3E0	BIT Interrupt Vector				
37E	Test (D2) verify	R/W	3B6	Module Design Revision	R	3E2	Over Current Interrupt Vector				
380	BIT Status Ch.1-10	R	3B8	Module DSP	R						
382	Over Current Status Ch.1-10	R	3BA	Module FPGA	R						
384	BIT Stat Interrupt Enable Ch.1-10	R/W	3BC	Module ID	R						
386	Over Current Interrupt Enable Ch.1-10	R/W									

(Filter Info In-Process)

Write D/A output

If using bi-polar mode, write 16 bit 2's complement word to the channel's *Data register* (7FFFh=+FS, 8000h=-FS) If using unipolar mode, write 16 bit binary word to the channel's *Data register* (range: 0 to FFFFh=FS).

D/A Output Polarity

Write integer 4 to the channel's *D/A Polarity register* for unipolar mode. Write integer 0 to the channel's *D/A range register* for bi-polar mode.

D/A Wrap-Around

Read D/A *wrap-around data* register, 16 bit 2's complement word (7FFFh=+FS, 8000h=-FS) bipolar mode, or 16 bit binary word (range 0 to FFFFh=FS)

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1"								ASCII " "								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "B"								ASCII " "								

Module DSP

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A

Read/Write: R
Initialized Value: 4E37h

Read register to determine Module ID in ASCII. For example, find ASCII "J" in upper byte and ASCII "7" in lower byte for Module "J7," together 4E37h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "J"								ASCII "7"								

BIT Status

Check the corresponding bit for a channel's BIT Status. A "0" =Normal; "1" = Non-compliant D/A conversion (outside 0.2% FS accuracy spec). Reading any status bit will cause that bit to be unlatched. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Current Reading

Current reading register allows for a general read on actual current being delivered per channel. Accuracy is approximately 5%. LSB is 1/10 ma.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Over Current Status

Check the corresponding bit of the *Over Current Status* registers for over current draw for each active channel. A "0" =Normal; "1" = Over Current. An over current draw from the output of any D/A channel is detected within 2 seconds and will latch the corresponding bit in the *Over Current Status* register. Reading any status bit will cause unlatch the entire register. Over Current Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status	X	X	X	X	X	X	Ch. 10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored for Over Current Status.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status Intr Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

D/A FIFO Buffer Operational Description

The D/A FIFO Buffering for greater control of the output voltage / signal (data). When the Buffer is enabled and triggered, the D/A buffer will accept / store / output the voltage for applications requiring simulation of waveform generation. The data can be "outputted" from the buffer at a maximum D/A Buffer base rate of 390.625 KHz or at the max base rate divided by an integer set in the Sample Rate Register. The thresholds of the buffer can be utilized for data flow control.

D/A Data:
The available data in the FIFO buffer can be retrieved in the following VME memory addresses one "WORD" (16bits) at a time. The data is presented in two's complement format depending on the range and polarity setting of the individual channel. For bipolar mode; 7FFFh=+FS, 8,000h=-FS. For unipolar mode, range is from 0h to FFFFh = FS.

Addr	r / w	Description	D/A Data(16Bit hex)
100	r	data ch1	Data Range: (0x0000-0xFFFF)
102	r	data ch2	
104	r	data ch3	
106	r	data ch4	
108	r	data ch5	
10A	r	data ch6	
10C	r	data ch7	
10E	r	data ch8	
110	r	data ch9	
112	r	data ch10	

Words in FIFO:
This is a counter that revolves the number of data in WORD (2 byte) stored in the FIFO buffer. Every time when a read operation is made to the D/A Data memory address, its corresponding "Words in FIFO" counter will be decremented by one. This register contains the number of data words in the buffer and is "dynamically" updated. The maximum number of words can be stored in the FIFO is 26,213(0x6665).

Addr	r / w	Description	Words in FIFO(16Bit hex)
120	r	Words in ch1	Data Range: (0x0000-0x6665)
122	r	Words in ch2	
124	r	Words in ch3	
126	r	Words in ch4	
128	r	Words in ch5	
12A	r	Words in ch6	
12C	r	Words in ch7	
12E	r	Words in ch8	
130	r	Words in ch9	
132	r	Words in ch10	

Hi-Threshold:

The Hi-Threshold level is a value used to set the high limit bit (B2) of the individual channel status register in VME memory location: 0x240 – 0x252. When the "Words in FIFO" counter is => than the value stored in the hi-threshold register, the high limit bit (B2) of the channel status register will be set. When the "Words in FIFO" counter is <= the value stored in the Lo-threshold register, the high limit bit (B2) of the channel status register will be reset (defaulted hysteresis).

Set = "logical 1"
Reset = "logical 0"

Addr	r / w	Description	Hi-Threshold(16Bit hex)
140	rw	Hi-Threshold in ch1	Data Range: (0x0000-0x6665)
142	rw	Hi-Threshold in ch2	
144	rw	Hi-Threshold in ch3	
146	rw	Hi-Threshold in ch4	
148	rw	Hi-Threshold in ch5	
14A	rw	Hi-Threshold in ch6	
14C	rw	Hi-Threshold in ch7	
14E	rw	Hi-Threshold in ch8	
150	rw	Hi-Threshold in ch9	
152	rw	Hi-Threshold in ch10	

Lo-Threshold:

The Lo-Threshold level is a value used to set or reset the low limit bit (B1) of the individual channel status register in VME memory location: 0x240 – 0x252. When the "Words in FIFO" counter is greater than or equal to the value stored in the Lo-Threshold, the low limit bit (B1) of the channel status register will be reset. When the "Words in FIFO" counter is less than the value stored in the Lo-Threshold, the low limit bit (B1) of the channel status register will be set. When the "Words in FIFO" counter is >= the value stored in the Hi-Threshold register, the high limit bit (B2) of the channel status register will be reset (defaulted hysteresis).

Set = "logical 1"
Reset = "logical 0"

Addr	r / w	Description	Low-Threshold(16Bit hex)
160	rw	Low-Threshold in ch1	Data Range: (0x0000-0x6665)
162	rw	Low-Threshold in ch2	
164	rw	Low-Threshold in ch3	
166	rw	Low-Threshold in ch4	
168	rw	Low-Threshold in ch5	
16A	rw	Low-Threshold in ch6	
16C	rw	Low-Threshold in ch7	
16E	rw	Low-Threshold in ch8	
170	rw	Low-Threshold in ch9	
172	rw	Low-Threshold in ch10	

Delay:

Set the number of delay samples (based on the sample rate) before the actual FIFO data is “outputted” after a trigger is initiated. This basically sets a delay time after trigger prior to “outputting” the data.

Addr	r / w	Description	Delay(16Bit hex)
180	rw	Delay in ch1	Data Range: (0x0000-0xFFFF)
182	rw	Delay in ch2	
184	rw	Delay in ch3	
186	rw	Delay in ch4	
188	rw	Delay in ch5	
18A	rw	Delay in ch6	
18C	rw	Delay in ch7	
18E	rw	Delay in ch8	
190	rw	Delay in ch9	
192	rw	Delay in ch10	

Size:

Set the size of the FIFO buffer. The largest size that a FIFO buffer can be is 26,213(0x6665)

Addr	r / w	Description	Size(16Bit hex)
1A0	rw	Size in ch1	Data Range: (0x0000-0x6665)
1A2	rw	Size in ch2	(If size is set to 0, the buffer will be read and “outputted”
1A4	rw	Size in ch3	after triggering. The user must insure (via threshold or
1A6	rw	Size in ch4	equivalent) that data is being “fed” to the buffer. If data
1A8	rw	Size in ch5	in the buffer empties, the channel will output the last
1AA	rw	Size in ch6	value.
1AC	rw	Size in ch7	
1AE	rw	Size in ch8	
1B0	rw	Size in ch9	
1B2	rw	Size in ch10	

Sample Rate:

The sample rate sets the "output update" rate for the FIFO buffer. The number entered in the Sample (update) Rate register will be the divisor of the actual Base D/A sample rate (Clock Rate Control). For example, the Base D/A Sample Rate is 390.625 KHz and the Sample Rate register is set to 2, then, after triggering, the output data rate will be 195312.5 KHz. For full Base D/A output rate from data stored in the buffer (390.625 KHz), the sampling rate would be set to "1".

Addr	r / w	Description	Sample Rate(16Bit hex)
1C0	rw	Rate in ch1	Data Range: (0x0001-0xFFFF)
1C2	rw	Rate in ch2	
1C4	rw	Rate in ch3	
1C6	rw	Rate in ch4	
1C8	rw	Rate in ch5	
1CA	rw	Rate in ch6	
1CC	rw	Rate in ch7	
1CE	rw	Rate in ch8	
1D0	rw	Rate in ch9	
1D2	rw	Rate in ch10	

Clear FIFO:

Whenever the Clear FIFO is set for the individual channel, it initializes the "Words in FIFO" to zero. A read to the A "write" of 0x0h initiates the clear. All the counters are reset and the output of the channel reverts back to whatever was set in the "DATA" register. To re-start the buffer output, the data would need to be re-loaded and re-triggered.

Addr	r / w	Description	Clear FIFO(16Bit hex)
1E0	rw	Clear in ch1	Data Range: (0x0000)
1E2	rw	Clear in ch2	
1E4	rw	Clear in ch3	
1E6	rw	Clear in ch4	
1E8	rw	Clear in ch5	
1EA	rw	Clear in ch6	
1EC	rw	Clear in ch7	
1EE	rw	Clear in ch8	
1F0	rw	Clear in ch9	
1F2	rw	Clear in ch10	

Buffer Control:

Defines the Buffer Operation Modes.

B0 = Buffer Enable

0 = Enable	Enables buffer data to be “outputted”, once triggered, at set sample rate and data size
1 = Disable	Disables Buffer Data “output”. Output is directly controlled from DATA register.

B1 = Mode Bit

0 = “1-Shot” Mode:	The data will be “outputted” from the FIFO Buffer, once triggered” at the set sample rate (and set sample rate) one time.
1 = “Repeat” Mode:	The data will be “outputted” from the FIFO Buffer, once triggered” at the set sample rate (and set sample size) and continuously repeat. Once disabled, the data will finish cycle and stay with output at last value.

B2 = Reserved
B3 = Reserved
B4 = Reserved
B5 = Reserved
B6 = Reserved
B7 = Reserved

Addr	r / w	Description	Buffer Ctrl.(16Bit hex)
200	rw	Buf. Ctrl. in ch1	Data Range: b0-b1
202	rw	Buf. Ctrl. in ch2	
204	rw	Buf. Ctrl. in ch3	
206	rw	Buf. Ctrl. in ch4	
208	rw	Buf. Ctrl. in ch5	
20A	rw	Buf. Ctrl. in ch6	
20C	rw	Buf. Ctrl. in ch7	
20E	rw	Buf. Ctrl. in ch8	
210	rw	Buf. Ctrl. in ch9	
212	rw	Buf. Ctrl. in ch10	

Trigger Control:

The FIFO can be started/triggered by different sources (either software control or via external pulse).

D0-D1 = Trigger Source Select (choose one only)

00 = Ext. Trigger 2
01 = Ext. Trigger 1
10 = Software Trigger

D2 = Reserved
D3 = Reserved

D4 = Slope (External Trigger)

0 = Positive Slope
1 = Negative Slope

D5 = Trigger Enable

0 = Trigger Disable
1 = Trigger Enable

D6 = Reserved

D7 = Trigger Clear (Stops from continuous trigger)
0 = Not Clear
1 = Clear
(Note: Must set back to "0" after clear to allow next trigger)

Set the bits for Trigger Control

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Trigger Control	X	X	X	X	X	X	X	X	Trigger Clear	X	Trigger Enable	Slope	X	X	Trigger Source	

Addr	r / w	Description	Trigger Ctrl.(16Bit hex)
220	rw	Trigger Ctrl. in ch1	Data Range: D0-D7
222	rw	Trigger Ctrl. in ch2	
224	rw	Trigger Ctrl. in ch3	
226	rw	Trigger Ctrl. in ch4	
228	rw	Trigger Ctrl. in ch5	
22A	rw	Trigger Ctrl. in ch6	
22C	rw	Trigger Ctrl. in ch7	
22E	rw	Trigger Ctrl. in ch8	
230	rw	Trigger Ctrl. in ch9	
232	rw	Trigger Ctrl. in ch10	

FIFO Status:
The FIFO status register indicates the current condition of the FIFO buffer. B0-B4 is used to show the different condition of the buffer.

B0 = Empty. When “Words In FIFO” register is zero, B0 = 1; otherwise =B0 =0.
B1 = Low Limit. When “Words In FIFO” register” < “Low-Threshold”, B1= 1; otherwise B1 =0.
B2 = High Limit. When “Words In FIFO” register” > “Hi-Threshold”, B2=1; otherwise B2 =0.
B3 = FIFO Full. When “Words In FIFO” register” = 26213, B3=1; otherwise B3 =0.
B4 = Sample Done. When “Words In FIFO” register = “Size”, B4=1; otherwise B4 =0.

Addr	r / w	Description	FIFO Status(16Bit hex)
240	r	FIFO Status in ch1	Data Range: b0-b4
242	r	FIFO Status in ch2	
244	r	FIFO Status in ch3	
246	r	FIFO Status in ch4	
248	r	FIFO Status in ch5	
24A	r	FIFO Status in ch6	
24C	r	FIFO Status in ch7	
24E	r	FIFO Status in ch8	
250	r	FIFO Status in ch9	
252	r	FIFO Status in ch10	

Interrupt Enable:

Interrupt(s) may be enabled based on the following;

B0 = Empty. When “Words In FIFO” register is zero, B0 = 1; otherwise =B0 =0.
B1 = Low Limit. When “Words In FIFO” register” < “Low-Threshold”, B1= 1; otherwise B1 =0.
B2 = High Limit. When “Words In FIFO” register” > “Hi-Threshold”, B2=1; otherwise B2 =0.
B3 = FIFO Full. When “Words In FIFO” register” = 26213, B3=1; otherwise B3 =0.
B4 = Sample Done. When “Words In FIFO” register = “Size”, B4=1; otherwise B4 =0.

Note: When/If an interrupt is enabled utilizing the low and high limit thresholds, the interrupt will not be “reset” or generate a new interrupt until the opposite threshold has been crossed (hysteresis). For example, if an interrupt enable is set for High Limit Threshold, once set, a new High Limit Threshold interrupt will not be generated until the Low Limit Threshold has been crossed.

Addr	r / w	Description	FIFO Status(16Bit hex)
260	rw	Interrupt Enable CH1	Data Range: b0-b4
262	rw	Interrupt Enable CH2	
264	rw	Interrupt Enable CH3	
266	rw	Interrupt Enable CH4	
268	rw	Interrupt Enable CH5	
26A	rw	Interrupt Enable CH6	
26C	rw	Interrupt Enable CH7	
26E	rw	Interrupt Enable CH8	
270	rw	Interrupt Enable CH9	
272	rw	Interrupt Enable CH10	

Software Trigger:

Software trigger is used to kick start the FIFO buffer and collection of data. In order to use this operation, the “Trigger Ctrl” register must be set up properly. Setting or resetting the “Software Trigger” will start FIFO data collection for ALL channels.

Addr	R / w	Description	Software Trigger(16Bit hex)
280	rw	Software Trigger	Data Range: 0x0-0xFFFF

Clock Rate Input
(Setting the BASE sample rate clock)

Utilize the Clock Rate Input Registers to set the actual or Base Sample Rate of the D/A (LSB of Clock Rate Input LO = 1 Hz). (32-bit word total)

For example, setting a Base Sample Rate of 44100 Hz would be set by initializing the Clock Rate Input HI and LO registers as such:

44100 = AC44(h);
REG 282 = 0000
REG 284 = AC44(h)

Setting a Base Sample Rate at the maximum 200 KHz would be set by initializing the Clock Rate Input HI and LO registers as such:

200000 = 30D40(h)
REG 282 = 0003(h)
REG 284 = 0D40(h)

Clock Rate Input Hi:

Addr	R / w	Description	Software Trigger(16Bit hex)
282	rw	Clk Rate Adder Input Hi	Data Range: 0x0-0xFFFF

Clock Rate Adder Low:

Addr	R / w	Description	Software Trigger(16Bit hex)
284	rw	Clk Rate Adder Input Low	Data Range: 0x0-0xFFFF

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
282	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
CLK Rate Input (HI)	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

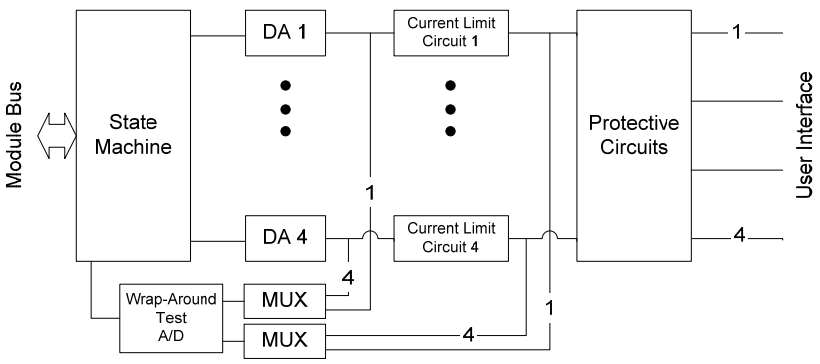
REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
284	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
CLK Rate Input (LO)	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	LSB=1Hz=DATA BIT=D

NOTE: Base Sample Rate Range (combined 32-bit word) 2000 to 200000.

HIGH VOLTAGE D/A (MODULE J8)

Four (4) D/A channels are provided per module and includes extensive diagnostics. To save power, DC-to-DC output drive is internally scaled according to programmed output range. Overloaded outputs will be detected, with the results displayed in a status word. This module incorporates major diagnostic capabilities that offer substantial improvements to system reliability because user is alerted to malfunctions within 5 seconds. Two different tests, one off-line (D2) and one on-line (D3) can be selected:

High Voltage DA Module Block Diagram



The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 2% FS and monitored for shorted output. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the operation of this card and can be enabled or disabled via the bus.

The (D3) test uses an internal A/D that measures all D/A channels while they remain connected to the I/O. Each channel will be checked to a test accuracy of 2% FS. Test cycle is completed within 45 seconds and results can be read from the Status registers when D3 changes from "1" to "0". The test can be stopped at any time. This test requires no user programming and can be enabled or disabled via the bus. **CAUTION:** D/A Outputs are active during this test. Check connected loads for interaction.

D/A Over Current (short circuit) monitoring is disabled during D3 testing.

MODULE MEMORY MAP

000	Data 1	R/W	014	Wrap-around 1	R/W	3B4	Module Design Version	R
002	Data 2	R/W	016	Wrap-around 2	R/W	3B6	Module Design Revision	R
004	Data 3	R/W	018	Wrap-around 3	R/W	3B8	Module DSP	R
006	Data 4	R/W	01A	Wrap-around 4	R/W	3BA	Module FGPA	R
008	Range 1 & 2	R/W	0D0	BIT Status Ch.1-4	R	3BC	Module ID	R
00A	Range 3 & 4	R/W	0D4	Over Current Status Ch.1-4	R			
00C	Polarity 1	R/W	0E8	BIT Stat Interrupt Enable Ch.1-4	R/W			
00E	Polarity 2	R/W	0EC	Over Current Interrupt Enable Ch.1-4	R/W			
010	Polarity 3	R/W						
012	Polarity 4	R/W						

Write D/A Output

If using bi-polar mode, write 16 bit 2's complement word to the channel's *Data register* (7FFFh=+FS, 8000h=-FS) If using unipolar mode, write 16 bit binary word to the channel's *Data register* (range: 0 to FFFFh=FS). Because output resolution is 12bits, enter LSBs D0 through D3 as zero. At power-on, output is initialized to 0 volts.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	0	0	0	0	D=DATA BIT

D/A Output Range

Program voltage range for channel pairs (1 & 2, or 3 & 4) from 20 to 90 volts. For 20 volts, enter integer 20. Resolution is 10 volts. 10 ma/channel maximum (source or sink) for up to 80VDC.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
										64	32	16	8	4	2	1	value in volts (LSB=1volt)
RANGE	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

0	**0**	**1**	**0**	**1**	**0**	**0**	20 volts
0	**0**	**1**	**1**	**1**	**1**	**0**	30 volts
0	**1**	**0**	**1**	**0**	**0**	**0**	40 volts
0	**1**	**1**	**0**	**0**	**1**	**0**	50 volts
0	**1**	**1**	**1**	**1**	**0**	**0**	60 volts
1	**0**	**0**	**0**	**1**	**1**	**0**	70 volts
1	**0**	**1**	**0**	**0**	**0**	**0**	80 volts

D/A Output Polarity

Write integer 4 to the channel's *D/A range register* for unipolar mode. Write integer 0 to the channel's *D/A range register* for bi-polar mode.

D/A Wrap-Around

Read D/A *wrap-around data* register, 16 bit 2's complement word (7FFFh=+FS, 8000h=-FS) bipolar mode, or 16 bit binary word (range 0 to FFFFh=FS)

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4A37h

Read register to determine Module ID in ASCII. For example, find ASCII "J" in upper byte and ASCII "1" in lower byte for Module "J7," together 4A37h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "J"								ASCII "7"								

BIT Status

Check the corresponding bit for a channel's BIT Status. A "0" =Normal; "1" = Non-compliant D/A conversion (outside 2% FS accuracy spec). Reading any status bit will cause that bit to be unlatched. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status

Check the corresponding bit of the *Over Current Status* registers for over current draw for each active channel. A "0" =Normal; "1" = Over Current. An over current draw from the output of any D/A channel is detected within 2 seconds and will latch the corresponding bit in the *Over Current Status* register. Reading any status bit will cause unlatch the entire register. Over Current Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

Over Current Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored for Over Current Status.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Over Current Status Intr Enable	X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

D/A (Module F5)	**Four (4) D/A Outputs ±20VDC at 100 mA, isolated from VME GND.**
Output range:	±20 VDC or 0 to 20 VDC, programmable. Output is set to 0 at reset or Power-on
Resolution:	16 bits/channel for either output range
Accuracy:	0.05% FS
Offset:	<1 mV over temperature
Non-linearity:	0.01% FS over temperature
Gain error:	0.02% over temperature
Output format:	Optically isolated in groups of ten (250 V to VME power)
Settling time:	10 μs max
Load:	100 ma/channel max.(Source or Sink). Can drive a capacitive load of 0.1 mfd. Short circuit protected. When current exceeds 110 ma for any channel, for >50ms, that channel is set to zero and a flag is set. Card is programmable to allow all channels to be reset by either an automatic retry or by a control port command.
Output impedance:	<1 Ω
Update rate:	5 microseconds per channel
ESD protection:	Designed to meet the testing requirements of IEC 801-2 Level 2. (4KV transient with a peak current of 7.5A and a time constant of approximately 60 ns
Power:	±12 VDC at 145 ma typical; 192 ma max. +5 VDC at 91 ma typical; 150 ma max
Weight:	1 oz. (28g)

D/A Reset to Zero

Write "1" to drive all D/A outputs to zero. When complete, *D/A Reset to Zero* register will be automatically set to "0".

D/A Retry Overload

Write "1" to *D/A Retry overload* register to enable all channels (board wide) whose outputs were previously set to zero caused by an overload condition. If an overload condition still exists, the channel output(s) will again be set to zero. While enabled, all overloaded channel outputs will be again be reset approx. every second. Default is "0".

D/A Reset Overload

This register is used to reset all channels whose outputs were previously set to zero because of an overload. If an overload condition still exists, channel output(s) will again be set to zero. Channel output reset will occur one time only. *D/A Reset overload* register is be automatically reset to 0 after channel output reset activity is complete. Card will attempt to reset channel output(s) once for every time "1" is written to the register.

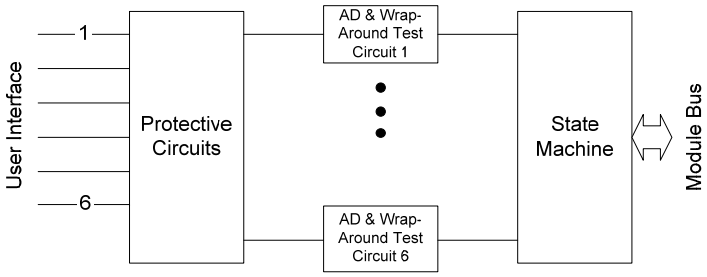
D/A Override

Write "1" at *Override* register to turn ON all overloaded outputs, short life condition.

RTD (MODULE G4)

The RTD channels use individual A/D converters. All RTD channels are self-calibrating because each channel, on a rotating basis, is automatically calibrated to eliminate offset and gain errors. The ability to set lower voltages for Full Scale Input, assures the utilization of the full resolution. Open inputs will be detected, with the results displayed in a status word. All inputs are double buffered for immediate availability. External excitation not required.

RTD Module Block Diagram



The (D2) test initiates **automatic** background BIT testing, where each channel is checked to a test accuracy of 0.2% FS and monitored for open input. Any failure triggers an Interrupt (if enabled) with the results available in status registers. The testing is totally transparent to the user, requires no external programming and has no effect on the operation of this card. It can be enabled or disabled via the bus.

RTD Open Circuit monitoring is disabled during D3 testing.

MODULE MEMORY MAP

000	Resistance 1	R	00C	Range 1	R/W	018	3 or 4 Wire Mode 1[1]	R/W	0D0	BIT Status Ch.1-6	R
002	Resistance 2	R	00E	Range 2	R/W	01A	3 or 4 Wire Mode 2[1]	R/W	0D2	Open Status Ch.1-6	R
004	Resistance 3	R	010	Range 3	R/W	01C	3 or 4 Wire Mode 3	R/W	0E8	BIT Stat Interrupt Enable Ch.1-6	R/W
006	Resistance 4	R	012	Range 4	R/W	01E	3 or 4 Wire Mode 4	R/W	0EA	Open Stat INTR Enable Ch.1-6	R/W
008	Resistance 5	R	014	Range 5	R/W	020	3 or 4 Wire Mode 5	R/W	3B4	Module Design Version	R
00A	Resistance 6	R	016	Range 6	R/W	022	3 or 4 Wire Mode 6	R/W	3B6	Module Design Revision	R
									3B8	Module DSP	R
									3BA	Module FPGA	R
									3BC	Module ID	R

Note: 1. For 3 or 4 Wire Modes, Consult Factory

Resistance

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Resistance measurement is a binary word and is dependant upon range.
For example, if the 0.01 ohms per count range is selected: 2710h x 0.01 = 10000 x 0.01 = 100 ohms.

The resistance/temperature relationship varies among RTDs and is function of its composite material (ex, Platinum, Copper, Nickel-Iron, Nickel, etc). An RTD's "Alpha" Temperature Coefficient and its nominal resistance (at say 0°C), while operating within its applicable resistance range, provide for a first order approximation.

For best accuracy, use resistance/temperature relationship provided by the RTD manufacture:

Select associated *Range* (0-655, or 1-2000)
Read *Resistance* and scale accordingly (0.01 Ω / bit , or 0.03 Ω / bit.)

Calculate temperature using RTD manufacture provided resistance/temperature relationship (a quadratic equation).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESISTANCE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Range

Type: 16 bit unsigned integer
Range: 0 or 1
Read/Write: R/W
Initialized Value: 0

Write “0” for a 0-655 ohm output range, 0.01 Ω / bit.
Write “1” for a 1-2000 ohm output range, 0.03 Ω / bit.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RANGE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

3 Wire Mode

Consult Factory.

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII “1” in upper byte and ASCII space in lower byte for Module Design Version “1 ” is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “1”								ASCII “ ”								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII “B” in upper byte and ASCII space in lower byte for Module Design Revision “B ” is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “B”								ASCII “ ”								

Module DSP

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Read register to determine Module ID in ASCII. For example, find ASCII “G” in upper byte and ASCII “1” in lower byte for Module “G1,” together 4731h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “G”								ASCII “1”								

BIT Status

Check the corresponding bit for a channel’s BIT Status. A “0” =Normal; “1” = Non-compliant A/D conversion (outside 0.2% FS accuracy spec). Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Open Status

Check the corresponding bit of the *Open Status* registers for open/disconnected RTD for each active channel.

“0” =Normal; “1” = Open (detected after 2 seconds). Reading any status bit will cause that bit to be unlatched. Open Status is part of background testing and the status register may be checked or polled at any given time.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status	X	X	X	X	X	X	Ch. 10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

BIT Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 00h to disable all channels.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

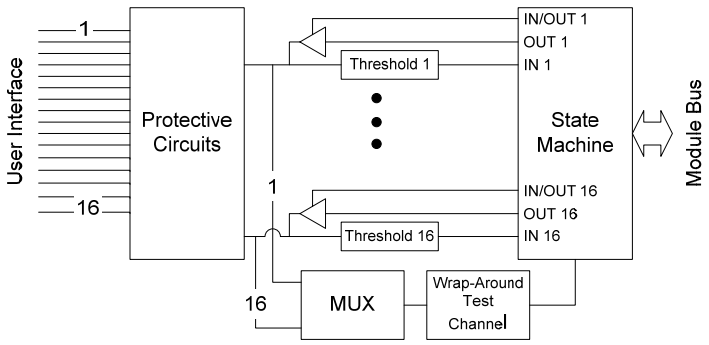
Open Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored for Open Status.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Open Status Interrupt Enable	X	X	X	X	X	X	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

I/O DISCRETE (MODULE K6)

Discrete IO Module Block Diagram



Each channel is programmable for either Input or Output. When programmed for Input, they can be used for either voltage or contact sensing. Voltage sensing covers the range of 0 to 80 VDC and offers four levels of switching thresholds. Channels set for contact sensing can be programmed for either pull-up or pull-down. Our unique design eliminates the need for pull-up resistors or mechanical jumpers. Instead, we offer a current source (in groups of 4) that user programs to a desired current level. When programmed for Output, each channel can be set for either High-side, Lo-side or Push-Pull operation. Diode clamping, useful for inductive loads, such as relays, and thermal protection are incorporated. Power isolated from the VME bus. There are 4 user provided Vcc inputs for each 16 channel module. There is one Vcc input for each four channel bank.

Module Memory Map

000	Write Output	Ch.01-16	R/W	04C	Upper Threshold	Ch.08	R/W	098	De-bounce time	Ch.15	R/W
002	Read I/O	Ch.01-16	R	04E	Lower Threshold	Ch.08	R/W	09A	Max High Threshold	Ch.16	R/W
004	Max High Threshold	Ch.01	R/W	050	Min Low Threshold	Ch.08	R/W	09C	Upper Threshold	Ch.16	R/W
006	Upper Threshold	Ch.01	R/W	052	De-bounce time	Ch.08	R/W	09E	Lower Threshold	Ch.16	R/W
008	Lower Threshold	Ch.01	R/W	054	Max High Threshold	Ch.09	R/W	0A0	Min Low Threshold	Ch.16	R/W
00A	Min Low Threshold	Ch.01	R/W	056	Upper Threshold	Ch.09	R/W	0A2	De-bounce time	Ch.16	R/W
00C	De-bounce time	Ch.01	R/W	058	Lower Threshold	Ch.09	R/W	0A4	Input/Output Format	Ch.01-08	R/W
00E	Max High Threshold	Ch.02	R/W	05A	Min Low Threshold	Ch.09	R/W	0A6	Input/Output Format	Ch.09-16	R/W
010	Upper Threshold	Ch.02	R/W	05C	De-bounce time	Ch.09	R/W	0A8	Current For Sink/Source, Bank 1	Ch.01-04	R/W
012	Lower Threshold	Ch.02	R/W	05E	Max High Threshold	Ch.10	R/W	0AA	Current For Sink/Source, Bank 2	Ch.05-08	R/W
014	Min Low Threshold	Ch.02	R/W	060	Upper Threshold	Ch.10	R/W	0AC	Current For Sink/Source, Bank 3	Ch.09-12	R/W
016	De-bounce time	Ch.02	R/W	062	Lower Threshold	Ch.10	R/W	0AE	Current For Sink/Source, Bank 4	Ch.13-16	R/W
018	Max High Threshold	Ch.03	R/W	064	Min Low Threshold	Ch.10	R/W	0B0	Pull Up/Down Current Config	Ch.01-16	R/W
01A	Upper Threshold	Ch.03	R/W	066	De-bounce time	Ch.10	R/W	0B4	Vcc Value, Bank 1	Ch.01-04	R
01C	Lower Threshold	Ch.03	R/W	068	Max High Threshold	Ch.11	R/W	0B6	Vcc Value, Bank 2	Ch.05-08	R
01E	Min Low Threshold	Ch.03	R/W	06A	Upper Threshold	Ch.11	R/W	0B8	Vcc Value, Bank 3	Ch.09-12	R
020	De-bounce time	Ch.03	R/W	06C	Lower Threshold	Ch.11	R/W	0BA	Vcc Value, Bank 4	Ch.13-16	R
022	Max High Threshold	Ch.04	R/W	06E	Min Low Threshold	Ch.11	R/W	0BC	Reset Over-Current	Ch.01-16	R/W
024	Upper Threshold	Ch.04	R/W	070	De-bounce time	Ch.11	R/W	0D0	Status Fault	Ch.01-16	R
026	Lower Threshold	Ch.04	R/W	072	Max High Threshold	Ch.12	R/W	0D4	Status Over-Current	Ch.01-16	R
028	Min Low Threshold	Ch.04	R/W	074	Upper Threshold	Ch.12	R/W	0D6	Status Max Hi Threshold	Ch.01-16	R
02A	De-bounce time	Ch.04	R/W	076	Lower Threshold	Ch.12	R/W	0D8	Status Min Lo Threshold	Ch.01-16	R
02C	Max High Threshold	Ch.05	R/W	078	Min Low Threshold	Ch.12	R/W	0DA	Status Mid Range	Ch.01-16	R
02E	Upper Threshold	Ch.05	R/W	07A	De-bounce time	Ch.12	R/W	0DC	Status Lo-Hi Transition	Ch.01-16	R
030	Lower Threshold	Ch.05	R/W	07C	Max High Threshold	Ch.13	R/W	0DE	Status Hi-Lo Transition	Ch.01-16	R
032	Min Low Threshold	Ch.05	R/W	07E	Upper Threshold	Ch.13	R/W	0E8	Interrupt Fault Enable	Ch.01-16	R/W
034	De-bounce time	Ch.05	R/W	080	Lower Threshold	Ch.13	R/W	0EC	Interrupt Over-Current Enable	Ch.01-16	R/W
036	Max High Threshold	Ch.06	R/W	082	Min Low Threshold	Ch.13	R/W	0EE	Interrupt Max Hi Threshold Enable	Ch.01-16	R/W
038	Upper Threshold	Ch.06	R/W	084	De-bounce time	Ch.13	R/W	0F0	Interrupt Min Lo Threshold Enable	Ch.01-16	R/W
03A	Lower Threshold	Ch.06	R/W	086	Max High Threshold	Ch.14	R/W	0F2	Interrupt Mid-Range Fault Enable	Ch.01-16	R/W
03C	Min Low Threshold	Ch.06	R/W	088	Upper Threshold	Ch.14	R/W	0F4	Interrupt Lo-Hi Transition Enable	Ch.01-16	R/W
03E	De-bounce time	Ch.06	R/W	8A	Lower Threshold	Ch.14	R/W	0F6	Interrupt Hi-Lo Transition Enable	Ch.01-16	R/W
040	Max High Threshold	Ch.07	R/W	08C	Min Low Threshold	Ch.14	R/W	3B4	Module Design Version		R
042	Upper Threshold	Ch.07	R/W	08E	De-bounce time	Ch.14	R/W	3B6	Module Design Revision		R
044	Lower Threshold	Ch.07	R/W	090	Max High Threshold	Ch.15	R/W	3B8	Module DSP		R
046	Min Low Threshold	Ch.07	R/W	092	Upper Threshold	Ch.15	R/W	3BA	Module FPGA		R
048	De-bounce time	Ch.07	R/W	094	Lower Threshold	Ch.15	R/W	3BC	Module ID		R
04A	Max High Threshold	Ch.08	R/W	096	Min Low Threshold	Ch.15	R/W				

Write Output

When a channel is configured for Output, write logic level High (“1”) or Low (“0”) to associated channel bit, in 16 bit binary word. Each bit corresponds to one of 16 channels (See Register Bit Map.) Output logic is defined by the provided Vcc voltage to that channel bank. There are four channels per bank (See J1 & J2, or P2 & P0 pin out.)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
WRITE OUTPUT	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

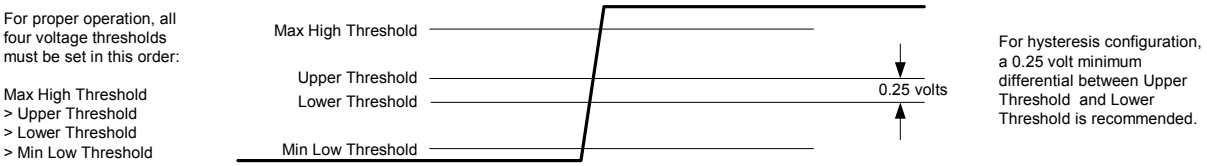
Read I/O

Independent of channel configuration (Input or Output), read logic state High (“1”) or Low (“0”) as defined by channel threshold values. Each bit of 16-bit binary word corresponds to one of 16 channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Channel
READ I/O	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

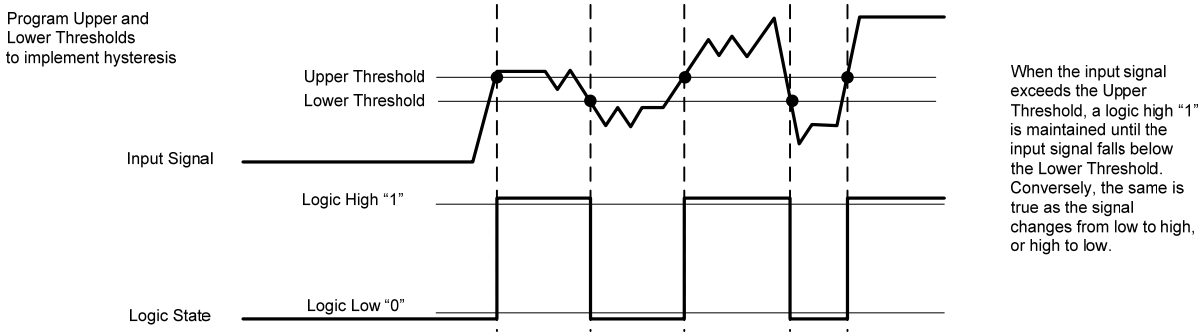
Threshold Programming

All four threshold levels must be programmed. For Input, threshold levels define logic. For output, threshold levels are used in BIT (wrap around) test signal monitoring. For proper operation, the threshold values should be programmed such that Max High > Upper > Lower > Min Low Threshold.



Hysteresis

Program Upper and Lower Thresholds to implement the required hysteresis and then add de-bounce time as required. When the input signal exceeds the Upper Threshold, a logic high “1” is maintained until the input signal falls below the Lower Threshold. Conversely, when the input signal falls below the Lower Threshold, a logic low “0” is maintained until the input signal rises above the Upper Threshold. A 0.25 volt minimum differential is recommended between the Upper and Lower Threshold values.



Max High Threshold

Maximum High Threshold is programmable per channel from 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv. Assumes that the programmed level is the minimum voltage used to indicate a Max HighThreshold. If a signal is greater then the Max High Threshold value, flag is set in the *Max High Threshold Status register*. The Max High Threshold register may be used to monitor any type of high signal voltage condition or threshold such as a “Short to +V” as it applies to input measurement as well as contact sensing applications.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
MAX HIGH THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

Upper Threshold

Upper Threshold is programmable per channel from 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv. A signal is considered logic High (“1”) when its value exceeds the Upper threshold and does not consequently fall below the Lower threshold in less than the programmed De-bounce time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
UPPER THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

Lower Threshold

Lower Threshold is programmable per channel from 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv. A signal is considered logic Low (“0”) when its value falls below the Lower threshold and does not consequently rise above the Upper Threshold in less than the programmed De-bounce time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
LOWER THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

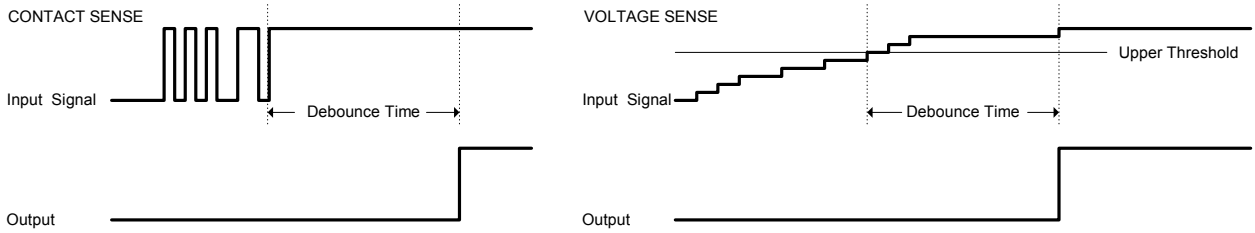
Min Low Threshold

Minimum Low Threshold is programmable per channel 0 VDC to 40 VDC. Binary 10 bit word, LSB=100 mv**.** Assumes that the programmed level is the maximum voltage used to indicate a Min Low Threshold. If a signal is less then the Min Low Threshold value, a flag is set in the *Min Low Threshold Status register*. The Min Low Threshold register may be used to monitor any type of low signal voltage condition or threshold such as a “Short to Ground” as it applies to input measurement as well as contact sensing applications.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	value in Volts (LSB=100mV)
MIN LOW THRESHOLD	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D=DATA BIT

De-bounce time

Enter required de-bounce time into appropriate channel registers. Enter time in 20μs increments, up to 0.655 seconds. LSB= 20 μs. Value is 15 bits (MSB=don’t care). De-bounce defaults to 0 upon reset. For contact sensing, De-bounce time is much like a glitch filter. Signal pulse widths less than the De-bounce time are filtered or ignored. Once a signal level is stable for a period longer than the De-bounce time (see Upper and Lower Threshold described above), a logic transition is validated. For voltage sensing, the input signal level must exceed its associated threshold for a time greater then the De-bounce time for the logic transition to be validated (see Upper and Lower Threshold described above). Once valid, the interrupt transition register channel flag is set and the output logic changes state. Enter a value of 0 to disable De-bounce filtering.



REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
		~328	~164	~82	40.96	20.48	10.24	5.12	2.56	1.28	0.64	0.32	0.16	0.08	0.04	0.02	value in mSec (LSB=20μS)
DE-BOUNCE TIME	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Input/Output Interface

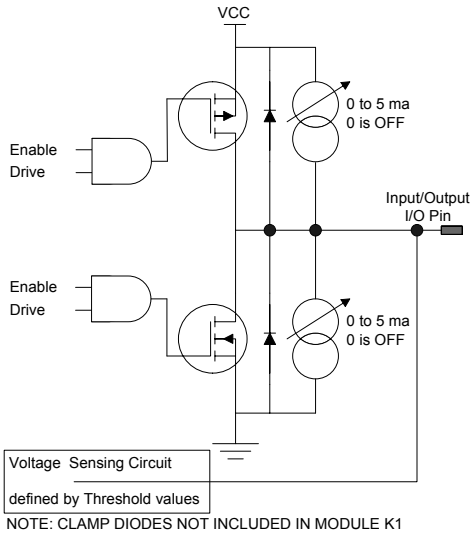
The Input/Output (I/O) Interface can be configured in a variety of ways. A pair of drive FETs and current circuits are provided at each I/O pin. See I/O interface diagram below.

Output: When configured as an output, the interface can act as a "High-Side", "Low-Side" or "Push-Pull" drive, providing up to 500ma per channel. The total output per module (16 channels) cannot exceed 2 amps.

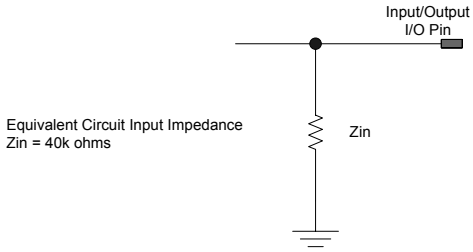
Input: When configured as an input, output drivers are disabled. I/O interface can act as a current source, current sink or voltage sensing circuit. For contact sensing, set each channel for pull-up or pull-down using the *Pull-Up/Down Current Configuration* register and enter the appropriate current level in the *Current For Sink/Source* register. Define contact closure and hysteresis using Upper and Lower Threshold. See *Read I/O* register to read input signal logic state. *No additional resistors or hardware is required to provide for current flow.* A current value of zero disables the current source/sink circuits and configures for voltage sensing. Default is voltage sensing.

All four threshold levels must be programmed. For input, threshold levels define logic state. For output, threshold levels are used in BIT test (wrap-around) signal monitoring.

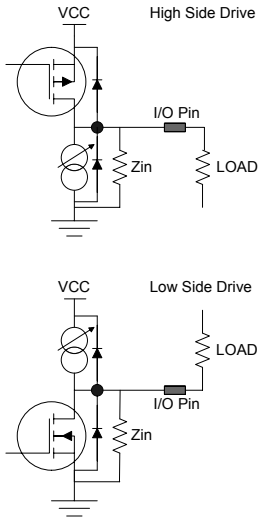
INPUT/OUTPUT INTERFACE

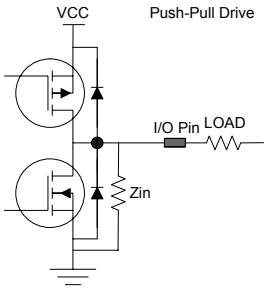


NOTE: CLAMP DIODES NOT INCLUDED IN MODULE K1

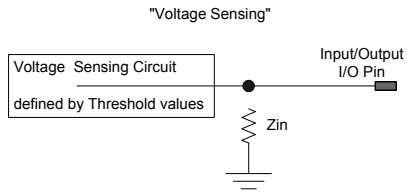


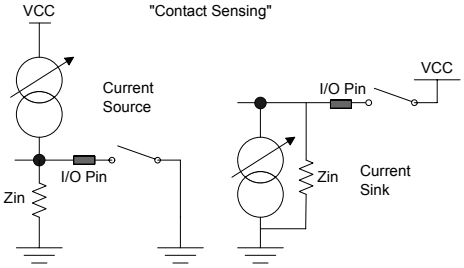
OUTPUT CONFIGURATIONS

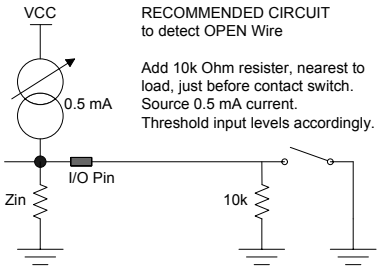




INPUT CONFIGURATIONS







To detect an OPEN line when **contact sensing,** add 10k ohm resistor R_{nl} nearest to load. Program open detect current I_{od} and calculate open contact condition, drop voltage V_{open} at I/O pin. Select sourcing current I_{od} such that drop voltage ΔV is about 80% of Vcc. If open detect resistance R_{od} is the parallel combination of the near load resistance R_{nl} and the circuit input impedance Z_{in}. Then

$R_{od} = R_{nl} \,||\, Z_{in}$ = 10k || 40k = 8k.

If user provided Vcc is 10v,

$I_{od} = 0.8\ Vcc / R_{od}$ = 0.8 x 10 / 8k = 1ma.

If I_{od} = 1ma, we get open contact condition, drop voltage V_{open} at the I/O pin,

$V_{open} = I_{od}R_{od}$ = 1ma x 8kΩ = 8.0 volts.

If load is current sink, Program Maximum Upper Threshold T_{mu}, some 20% greater then V_{open} , maintaining

$Vcc > T_{mu} > V_{open} > T_{ut}$,

T_{mu} = 1.2 V_{open} = 1.2 x 8 = 9.6 volts.

Program Upper Threshold T_{ut} 20% less then V_{open}

T_{ut} = 0.8 V_{open} = 0.8 x 8 = 6.4 volts.

Accordingly, program Lower Threshold T_{lt} at 20% Vcc and Minimum Lower Threshold T_{ml} at 10% Vcc

T_{lt} = 0.2 Vcc = 0.2 x 10 = 2 volts.
T_{ml} = 0.1 Vcc = 0.1 x 10 = 1 volts.

To detect a line SHORT when **contact sensing** and continuing with this example, user needs to add series resistance nearest to load, Rs and calculate closed contact condition, drop voltage V_{closed} at I/O pin. Resistance nearest to load, R_s should be negligible as compared to the near load resistance R_{nl} but at least a magnitude greater than any resistance due to wire length. A value of 150 ohms would be appropriate for Rs. Then

$V_{closed} = I_{od}R_s$ = 1ma x 0.1kΩ = 0.15 volts.

Program Lower Threshold T_{mu}, greater then V_{closed} maintaining

$Vcc >> T_{lt} > V_{closed} > T_{ml} > 0$

T_{lt} > 1.2 V_{closed} > 1.2 x 0.1 = 0.2 volts.

Program Minimum Lower Threshold T_{ut} 20% less then V_{open}

T_{ml} < 0.8 V_{closed} < 0.8 x 0.15 = 0.1 volts.

In general,

$Vcc > T_{mu} > V_{open} > T_{ut}, > T_{lt} > V_{closed} > T_{ml} > 0,$ $T_{ut} - T_{lt} \geq 0.25mV$ for hysteresis configuration

To detect a Short to Vcc, Program Maximum Upper Threshold T_{mu}, where

$Vcc > T_{mu} > V_{loadmax}$, where $V_{loadmax}$ is the maximum voltage potential on the I/O pin.

To detect a Short to Ground, Program Minimum Lower Threshold T_{ml}, where

$Vcc > > V_{loadmin} > T_{ml}$, where $V_{loadmin}$ is the minimum voltage potential on the I/O pin.

Consider the following programming options:

Output Programming Examples:

Figure	INPUT/OUTPUT FORMAT 2 bits per channel	Integer	PULL-UP/DOWN Configuration 1 bit per 4-channel bank	Integer	CURRENT FOR SOURCE/SINK One register per 4-channel bank	Integer
1	Output Ch1, High Side Drive	2	without current pull down	X	NO current source	0
1	Output Ch1-4, High Side Drive	170	Ch1-4 with current pull down[1]	14	1 ma	10
1	Output Ch5-8, High Side Drive	43520	Ch5-8 with current pull down[1]	13	2 ma	20
1	Output Ch1-8, High Side Drive	43690	Ch1-8 with current pull down[1]	12	2 ma	20
2	Output Ch1, Low Side Drive	1	without current pull up	X	NO current source	0
2	Output Ch1-4, Low Side Drive	85	Ch1-4 with current pull up[1]	1	1 ma	10
2	Output Ch1-8, Low Side Drive	21845	Ch1-8 with current pull up[1]	3	2 ma	20
3	Output Ch1, Push-Pull	3	Not Applicable – DON'T CARE	X	Not Applicable – DON'T CARE	X

Note 1: Use current source for Wired-OR or other related applications.

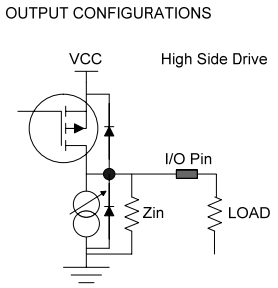


Figure 1

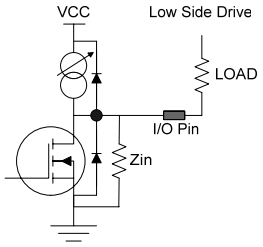


Figure 2

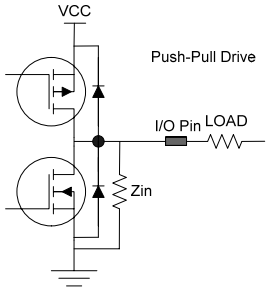


Figure 3

Input Programming Examples:

Figure	INPUT/OUTPUT FORMAT 2 bits per channel	Integer	PULL-UP/DOWN Configuration 1 bit per 4-channel bank	Integer	CURRENT FOR SOURCE/SINK One register per 4-channel bank	Integer
4	Input Ch1-8, voltage sensing (default)	0	without current source/sink	X	NO current source (default)	0
5	Input Ch1-8, contact sensing	0	Ch1-8 with current pull up	3	1 ma	10
6	Input Ch1-8, contact sensing	0	Ch1-8 with current pull down	12	2 ma	20
7	Input Ch1-8, OPEN line detect, load is current sink	0	Ch1-8 with current pull up	3	0.5 ma Program Max Upper Threshold[2]	5
6[1]	Input Ch1-8, OPEN line detect, load is current source	0	Ch1-8 with current pull down	12	0.5 ma Program Min Lower Threshold[3]	5

Notes 1. Figure 6 with 10k ohm resistor nearest load (as in figure 7)

2. $Vcc > T_{mu} > I_{od}R_{od}$, where load is current sinking

3. $T_{ml} < Vcc - I_{od}R_{od}$, where load is current sourcing

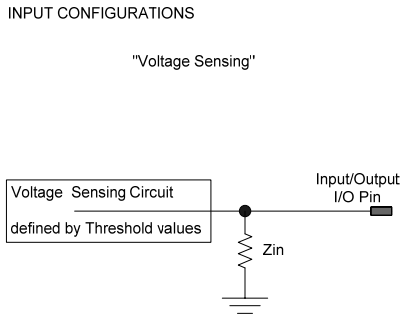


Figure 4

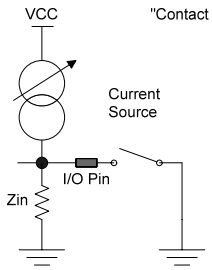


Figure 5

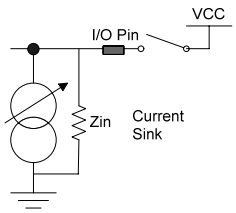


Figure 6

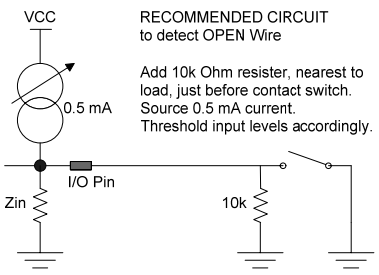


Figure 7

Current for Source/Sink

Program any current from 0 to 5 ma. Programs entire bank; there are 4 channels per bank. For 5ma, enter integer 50. Resolution is 100µa per bit (LSB=100µa). A current value of zero disables the current source/sink circuits and configures for voltage sensing.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
											3.2	1.6	0.8	0.4	0.2	0.1	value in mA (LSB=100µA)
CURRENT	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Input/Output format

Configure channels in groups of 8. Write integer 0 for input, 1, 2 or 3 for output. While each channel may be programmed for either input or output individually, Pull-up/down Current Configuration must be programmed in four channel banks.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INPUT/OUTPUT CH 01-08	Ch.08		Ch.07		Ch.06		Ch.05		Ch.04		Ch.03		Ch.02		Ch.01		Channel
INPUT/OUTPUT CH 09-16	Ch.16		Ch.15		Ch.14		Ch.13		Ch.12		Ch.11		Ch.10		Ch.09		Channel
INPUT/OUTPUT	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D_H	D_L	D=DATA BIT

Integer	D_H	D_L	
0	**0**	**0**	Input
1	**0**	**1**	Output, Low-side switched, with/without current pull up
2	**1**	**0**	Output, High-side switched, with/without current pull down
3	**1**	**1**	Output, push-pull

Pull-up/down Current Configuration

Set bit "1"=to configure Bank to Pull-up, or clear bit "0" to configure Bank to Pull-down. Each data bit configures entire bank of 4 channels. Defaults to "1"; pull-up configuration. Register data bits D4 through D15 are "don't care": XXXX XXXX XXXX $D_3D_2D_1D_0$

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
VCC VALUE	X	X	X	X	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	1=Pull-Up, 0=Pull-Down
D0 configures bank 1, channels 1-4 of that module.																**D**	Configure Ch.01-04
D1 configures bank 2, channels 5-8 of that module.															**D**		Configure Ch.05-08
D2 configures bank 3, channels 9-12 of that module.														**D**			Configure Ch.09-12
D3 configures bank 4, channels 13-16 of that module.													**D**				Configure Ch.13-16

Examples: Register value is integer:

Register Value	Data Bits			Channel Configuration, Module 1		
	D15-D2	D1	D0	Ch. 9-16	Ch. 5-8	Ch. 1-4
0	**0000 0000 0000 00 - -**	**0**	**0**	Pull-Down	Pull-Down	Pull-Down
1	**0000 0000 0000 00 - -**	**0**	**1**	Pull- Down	Pull-Down	Pull-Up
2	**0000 0000 0000 00 - -**	**1**	**0**	Pull- Down	Pull-Up	Pull-Down
3	**0000 0000 0000 00 - -**	**1**	**1**	Pull- Down	Pull-Up	Pull-Up

Vcc Value

Read Vcc voltage at input pin per four channel bank. Value is binary 10 bit word, where LSB=100 mv. Whether configured for input or output, user provided Vcc must be wired for proper operation.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
								25.6	12.8	6.4	3.2	1.6	0.8	0.4	0.2	0.1	value in volts (LSB=100mv)
VCC VALUE	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Reset Over-Current

Write integer "1" to reset all sixteen channels (per module). This register is used to reset disabled channel(s) set to tri-state following an over-current condition. When reset process is complete, processor will write a "0" back to the *Reset Over-Current* register. Card will respond to a Reset command after one second.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RESET OVER-CURRENT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**D**	D=DATA BIT

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "1"								**ASCII " "**								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII "B"								**ASCII " "**								

Module DSP

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Module FPGA

Type: binary word
Range: 0 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 4B31h

Read register to determine Module ID in ASCII. For example, find ASCII “K” in upper byte and ASCII “1” in lower byte for Module “K1,” together 4B31h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “K”								ASCII “1”								

L(R)VDT (MODULE L*)

Automatic background BIT testing

BIT is always enabled and continually checks that each channel is functional. This capability is accomplished by an additional Test A/D that is incorporated into each 16 channel module. The Test A/D is sequentially connected across each channel and compared against the operational channel. Depending upon configuration, the Input data read or Output logic write of the operational channel and Test A/D must agree or a fault is indicated with the results available in the associated status register. Additional testing is provided to check for Over-current condition. *All four threshold levels must be set for each Input or Output channel to validate BIT testing*. The card will write 55h to the *Test (D2) Register*, every 30 seconds. User can periodically clear the *Test (D2) Register* by writing 00h, waiting 30 seconds then reading the register again to verify that background BIT testing is functioning. Testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and associated status register(s) can be checked or polled at any given time. Enable Interrupts, within any interrupt enable register, by setting the appropriate channel bits to 1.

Status indications

Fault – Channel processing (data read or write logic) is inconsistent with redundant test circuit. Status (bit is set) is indicated within 15 seconds. A fault is latched until read. (Testing takes approx. 1 second per channel)

Over-current – If over-current or overload condition is sensed, status is indicated (bit is set) within 80µs.
Max High Threshold – If the signal exceeds this threshold, status is indicated (bit is set) within 40µs.
Min Low Threshold – If the signal falls below this threshold, status is indicated (bit is set) within 40µs.
Lo-Hi Transition – If a Lo to High transition is sensed, status is indicated (bit is set) within 40µs.
Hi-Low Transition – If a High to Low transition is sensed, status is indicated (bit is set) within 40µs.
Mid-Range – When the signal is in-between the Upper and Lower thresholds, status is indicated (bit set) within 40µs.

When status is “indicated,” or bit is “set,” bit value is logic “1.” Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Max Hi Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Min Lo Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Mid-Range	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Max Hi Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Min Lo Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Mid-Range Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Status Interrupt Enable

Set the bit to enable interrupts for the corresponding channel monitored. When status is “indicated,” or bit is “set,” bit value is logic “1.” Reading will reset (or unlatch) Status Register.

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status Fault	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Over-Current	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Max Hi Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Min Lo Threshold	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Mid-Range	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Lo-Hi Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Status Hi-Lo Transition	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Fault Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Over-Current Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Max Hi Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Min Lo Threshold Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Mid-Range Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Lo-Hi Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1
Interrupt Hi-Lo Enable	Ch.16	Ch.15	Ch.14	Ch.13	Ch.12	Ch.11	Ch.10	Ch.9	Ch.8	Ch.7	Ch.6	Ch.5	Ch.4	Ch.3	Ch.2	Ch.1

Principals of LVDT Operation :

Typically the LVDT primary is excited by an ac source, causing a magnetic flux to be generated within the transducer. Voltages are induced in the two secondaries, with the magnitude varying with the position of the core. Usually, the secondaries are connected in series opposition, causing a net output voltage of zero when the core is at the electrical center. When the core is displaced in either direction from center the voltage increases linearly either in phase or out of phase with the excitation depending on the direction.

Interfacing the LVDT to the Converter

Two common connection methods are:

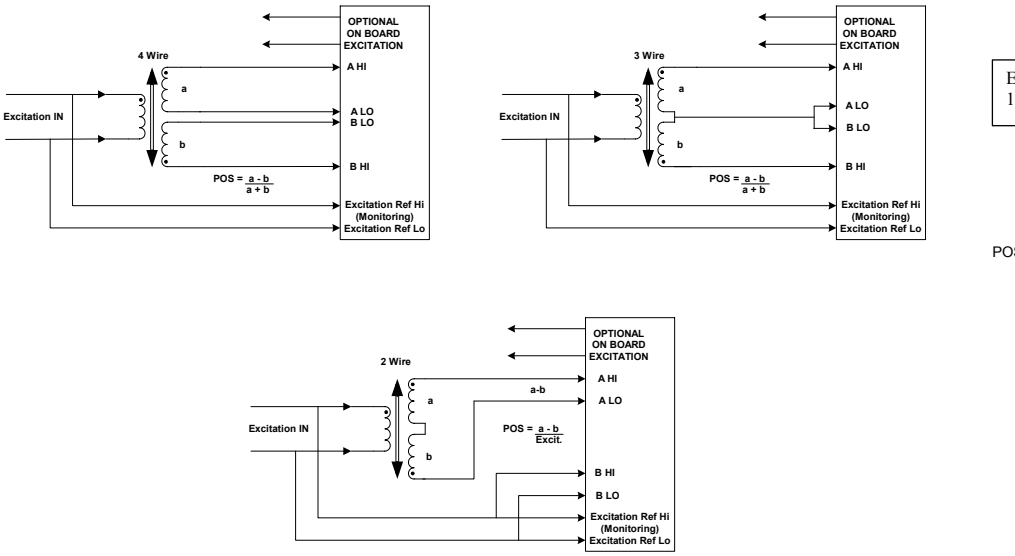
Primary as reference (two-wire system)

This method of connection converts the widest range of LVDT sensors and is the most sensitive to excitation voltage variations, temperature and phase shift effects.

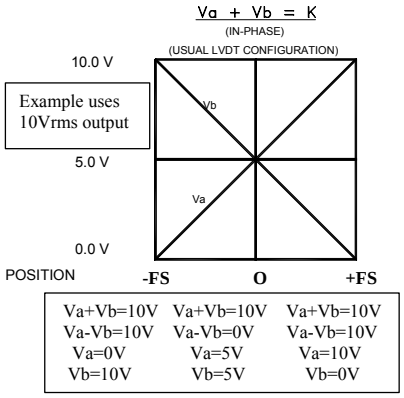
Derived reference (three/four-wire LVDT)

The LVDT is again excited from the primary side, but the converter reference is the sum of A + B that has constant amplitude for changing core displacement. This system is insensitive to temperature effects, phase shifts and oscillator instability and solves the identity (A-B) / (A+B)

Various LDVT configurations



LVDT Coil Voltage vs. Position



LVDT Connections:

For 3,4 Wire LVDT's, connect A and B LVDT outputs to Signal A and B inputs. Excitation is not used, but should be connected to allow card to monitor and report any excitation loss.

For 2 Wire LVDT's, connect A-B output of LVDT to card "A" input and connect external excitation voltage to card "B" input and to excitation input to allow card to monitor and report any excitation loss.

PROGRAMMING INSTRUCTIONS:

MEMORY MAP

00	Ch.1	read	44	Scale Ch.3	read/write	A8	(A+B) Ch.5	read	CE	Interrupt Level	write/read
02	Ch.2	read	46	Scale Ch.4	read/write	AA	(A+B) Ch.6	read	D0	2 or 3,4 wire input	write/read
04	Ch.3	read	48	Scale Ch.5	read/write	AC	(A+B) Ch.7	read	D2	Interrupt Vector 1	write/read
06	Ch.4	read	4A	Scale Ch.6	read/write	AE	(A+B) Ch.8	read	D6	Test (D2) verification	write/read
08	Ch.5	read	4C	Scale Ch.7	read/write	B0	(A+B) Ch.9	read	D8	Status, Signal	read
0A	Ch.6	read	4E	Scale Ch.8	read/write	B2	(A+B) Ch.10	read	DA	Status, Test	read
0C	Ch.7	read	50	Scale Ch.9	read/write	B4	(A+B) Ch.11	read	DC	Status, Exc.	read
0E	Ch.8	read	52	Scale Ch.10	read/write	B6	(A+B) Ch.12	read	DE	Latch	write
10	Ch.9	read	54	Scale Ch.11	read/write	C0	Active Channels	write/read	E0	Part #	read
12	Ch.10	read	56	Scale Ch.12	read/write	C2	Save	write/read	E2	Serial Number	read
14	Ch.11	read	A0	(A+B) Ch.1	read	C4	Internal Excitation Freq.	read/write	E4	Date code	read
16	Ch.12	read	A2	(A+B) Ch.2	read	C6	Internal Excitation Eo	read/write	E6	Rev level	read
40	Scale Ch.1	read/write	A4	(A+B) Ch.3	read	CA	Test Enable	write/read			
42	Scale Ch.2		A6	(A+B) Ch.4	read	CC	Test position	write			

REGISTER BIT MAP

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Latch Outputs	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0
Active channels	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	X	X	X	X
Status, Test	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	X	X	X	X
Status, Signal	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	X	X	X	X
Status, Excitation	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	X	X	X	X
2 or 3,4 wire Input	Ch.1	Ch.2	Ch.3	Ch.4	Ch.5	Ch.6	Ch.7	Ch.8	Ch.9	Ch.10	Ch.11	Ch.12	X	X	X	X

Irrespective of the method of connection, the codes will be 2's complement.
At **Power-On** or **System Reset**, all parameters are restored to factory default values.

Active Channels: Set the bit, corresponding to each channel to be monitored during BIT testing, in the *Active Channel Register*. "1"=active; "0"=not used. Omitting this step will produce false alarms because unused channels will set faults.

Interrupt Level: Enter interrupt level in the *Interrupt Level Register* as a 16-bit binary number.
0 = no interrupt; 1-7 indicates priority levels.

Interrupt Vector 1: Write an 8-bit word (0-255) to the *Interrupt Vector 1 Register*. Used for failure reports.

Selecting 2 or 3,4 Wire operation: Program the corresponding bit for the appropriate channel in the *2 or 3/4 Wire Input Register*. Logic 1 = 2 wire; logic 0 = 3 or 4 wire.

Data Format:
For 4-wire or 3-wire inputs, the output data is A-B/A+B and represents %FS. Format is two's complement. Maximum positive excursion is 32767 (7FFFh), 0 = 0, and maximum negative excursion is –32768 (8000h).

For 2-wire input, the output data is A-B/Excitation and represents %FS. Format is two's complement. Maximum positive excursion is 32767 (7FFFh), 0 = 0, and maximum negative excursion is –32768 (8000h).

Programming Position Scale Registers

The 4-wire or 3-wire LVDT has two output voltages referred to as A and B. When connected to the A and B Signal inputs, no scaling is required because the inputs are auto-ranging, however the corresponding *Position Scale Register* can be used to scale the output code.

Default settings for the *Position Registers* are 65535 (FFFFh) which results in a full-scale output reading for full travel of the LVDT. A full-scale output reading for less than full travel of the LVDT can be obtained by writing a scale value to the corresponding *Position Register*. For example, writing 32768 (8000h) to address *Position Scale Chan 1 Register* will result in channel 1 having a full-scale output reading for one-half travel of the LVDT.

For 2-wire input, the default settings for the *Signal Registers* are 65535 (FFFFh), which result in a full-scale output reading for full travel of the LVDT for TR = 1 (transformer ratio). To achieve full output readings for TR < 1, a scale factor (SF) should be programmed into the corresponding *Signal Register*. This is calculated from the equation:

$$SF = 65535\ (FFFFh) \times TR$$

The calculated SF value is written to the corresponding *Position Scale Register.*

Read (A+B) Output: Read binary number and multiply by 0.01 Volt. Only valid for 3 or 4 wire configurations.

Latch: All channels may be latched by writing a "1" to D1 in the *Latch Register*. Reading a particular channel will disengage the latch for that channel. Writing a 0 to this register will disengage latch on all channels.

D2 Test Enable: Writing a "1" to the D2 bit of the *Test Enable Register***,** initiates automatic background BIT testing. Each channel is checked over the programmed Signal range to a measuring accuracy 0.1%FS. An Interrupt will be set to indicate an accuracy problem. A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. The results are available in *Test Status Register*. The card will write 55h to the *Test (D2) Verification Register* when D2 is enabled. User can periodically clear to 00h and then read the *Test (D2) Verification Register* again, after 30 seconds, to verify that background BIT testing is activated.

In addition, each Signal and Excitation input is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *Signal* and *Excitation Status Registers*.

Status, Test: Check the channel's corresponding bit of the *Test Status Register* for status of BIT testing for each active channel. A "1" =Accuracy OK; "0" =failed. Channels that are inactive are also set to "0". (Test cycle takes 45 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the Test Status Register. Reading will unlatch register.

Status, Exc: Check the channel's corresponding bit of the *Excitation Status Register*, for status of the excitation input for each active channel. A "1" = Excitation. ON, "0" = Excitation. loss. Channels that are inactive are also set to "0".(Excitation loss is detected after 2 seconds). Excitation monitoring is disabled during D3 or D0 Test. Any Excitation status failure, transient or intermittent will latch the *Excitation Status Register*. Reading will unlatch register.

Status, Sig: Check the channel's corresponding bit of the *Signal Status Register*, for status of the input signals for each active channel. A "1" = Signal ON, "0" = Signal loss. Channels that are inactive are also set to "0". (Signal loss is detected after 2 seconds). Any Signal status failure, transient or intermittent will latch the *Signal Status Register*. Reading will unlatch register.

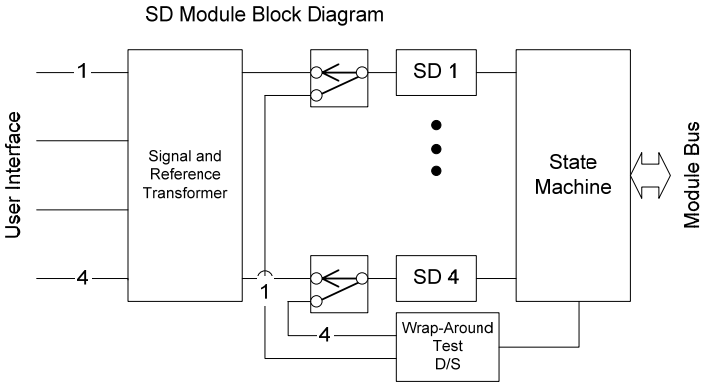
D3 Test Enable: Power-on Self-Test (POST), if enabled, or writing a "1" to D3 in the *Test Enable Register*, starts an initiated BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates multiple test voltages that are measured to a test accuracy of 0.1%FS. Test cycle takes about 10 seconds and results can be read from the Test Status Register when D3 changes from "1" to "0". External excitation is not required. An Interrupt, if enabled will be generated if a BIT failure is detected (See *Interrupt Register*). Testing requires no external programming and can be terminated by writing "0" to D3 of the *Test Enable Register*.

Signal and Excitation monitoring is disabled during D3 test.

D0 Test Enable: Checks the card and the VME interface. Writing a "1" to D0 in the *Test Enable Register* disconnects all channels from the outside world, allowing user to write any number of input positions to the card in the *Test Position Register* and then reads the data from the VME interface (allow 50 ms after writing). External excitation is not required.

Signal and Excitation monitoring is disabled during D0 test.

S/D (MODULE S*)



This S/D measurement design has the capability to automatically shift to higher bandwidths when high acceleration events are encountered. There is not data latency. The shifting is smooth and continuous with no glitches. Tracking rates are only limited to bandwidth restrictions, up to 150 RPS, at 16-bit resolution. Both a software and hardware LATCH feature is provided to permit the user to read all channels at the same time. Reading will unlatch that channel. The angle alert monitors each channel for the programmed angle difference and sets an interrupt as soon as that threshold is reached. Thus, no polling of the angle registers is required until an angle has reached the specified difference. The use of Type II servo loop processing techniques enables tracking, at full accuracy, up to the specified rate. A step input will not cause any hang-up condition. Intermediate transparent latches, on all angle and velocity outputs, assure that valid data is always available. Our synthetic reference compensates for ±60° phase shifts, thus eliminating the need for individual compensation networks.

The (D2) Test initiates automatic background BIT testing. Each channel is checked every 5° to a testing accuracy of 0.05° and each Signal and Reference is always monitored. Any failure triggers an Interrupt (if enabled) and the results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of the card, and can be enabled or disabled via the bus.

The (D3) Test initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. Results can be read from registers and external reference is not required. Any failure triggers an Interrupt (if enabled). The testing requires no external programming, and can be initiated or stopped via the bus.

The (D0) Test is used to check the card and the VME interface. All channels are disconnected from the outside world, allowing the user to write any number of input angles to the card and then to read the data from the interface. External reference is not required.

S/D MEMORY MAP

000	SD1 Data Lo	R	070	SD1 Encoder Resolution	W/R	320	CH1 Data Buffer HI Watermark	W/R
002	SD1 Data Hi	R	072	SD2 Encoder Resolution	W/R	322	CH1 Data Buffer Lo Watermark	W/R
004	SD2 Data Lo	R	074	SD3 Encoder Resolution	W/R	324	CH1 Buffer Delay Sample	W/R
006	SD2 Data Hi	R	076	SD4 Encoder Resolution	W/R	326	CH1 Buffer # of Samples	W/R
008	SD3 Data Lo	R	080	SD1 Signal Loss Threshold	W/R	328	CH1 Buffer Sample Rate	W/R
00A	SD3 Data Hi	R	082	SD2 Signal Loss Threshold	W/R	32A	CH1 Buffer Data Type	W/R
00C	SD4 Data Lo	R	084	SD3 Signal Loss Threshold	W/R	32C	CH1 Buffer Trigger Mode	W/R
00E	SD4 Data Hi	R	086	SD4 Signal Loss Threshold	W/R	330	CH2 Data Buffer HI Watermark	W/R
010	SD1 VEL Lo	R	088	SD1 REF Loss Threshold	W/R	332	CH2 Data Buffer Lo Watermark	W/R
012	SD1 VEL HI	R	08A	SD2 REF Loss Threshold	W/R	334	CH2 Buffer Delay Sample	W/R
014	SD2 VEL Lo	R	08C	SD3 REF Loss Threshold	W/R	336	CH2 Buffer # of Samples	W/R
016	SD2 VEL HI	R	08E	SD4 REF Loss Threshold	W/R	338	CH2 Buffer Sample Rate	W/R
018	SD3 VEL Lo	R	0A8	SD1 VEL SCALE	W/R	33A	CH2 Buffer Data Type	W/R
01A	SD3 VEL HI	R	0AA	SD2 VEL SCALE	W/R	33C	CH2 Buffer Trigger Mode	W/R
01C	SD4 VEL Lo	R	0AC	SD3 VEL SCALE	W/R	3B4	Module Design Version	
01E	SD4 VEL HI	R	0AE	SD4 VEL SCALE	W/R	3B6	Module Design Revision	
020	SD1 Bandwidth	R/W	0E8	SIG Status Ch.1-4	R	3B8	Module DSP Rev	W/R
022	SD2 Bandwidth	R/W	0EA	REF Status Ch.1-4	R	3BA	Module FPGA Rev	W/R
024	SD3 Bandwidth	R/W	0EC	BIT Status Ch.1-4	R	3BC	Module ID	R
026	SD4 Bandwidth	R/W	0EE	SD Lock Status Ch.1-4	R			
028	Bandwidth Select	R/W	0F0	SD Angle Δ Status Ch.1-4	R			
02A	SD Ratio 1/2	R/W	0F2	SIG Status Interrupt Enable Ch.1-4	R/W			
02C	SD Ratio 3/4	R/W	0F4	REF Status Interrupt Enable Ch.1-4	R/W			
02E	SD Active Channels	R/W	0F6	BIT Status Interrupt Enable Ch.1-4	R/W			
030	SD Track / Hold	R/W	0F8	SD Lock Status Interrupt Enable Ch.1-4	R/W			
032	D2 Test Verify	R/W	0FA	SD Angle Δ Interrupt Enable Ch.1-4	R/W			
034	Test Enable	R/W	100	OSC Freq Lo	W/R			
036	Test Angle	R/W	102	OSC Freq HI	W/R			
03E	SD SYN/RSL SELECT	R/W	104	OSC Volt Lo	W/R			
040	SD1 Angle Δ	R/W	106	OSC Volt Hi	W/R			
042	SD2 Angle Δ	R/W	200	Vector Signal Loss	W/R			
044	SD3 Angle Δ	R/W	202	Vector REF Loss	W/R			
046	SD4 Angle Δ	R/W	204	Vector BIT Fail	W/R			
04E	Angle Δ INIT	R/W	206	Vector Lock Loss	W/R			
050	SD1 Frequency LO	R	208	Vector Angle Δ	W/R			
052	SD1 Frequency HI	R	340	CH3 Data Buffer HI Watermark	W/R			
054	SD2 Frequency LO	R	342	CH3 Data Buffer Lo Watermark	W/R			
056	SD2 Frequency HI	R	344	CH3 Buffer Delay Sample	W/R			
058	SD3 Frequency LO	R	346	CH3 Buffer # of Samples	W/R			
05A	SD3 Frequency HI	R	348	CH3 Buffer Sample Rate	W/R			
05C	SD4 Frequency LO	R	34A	CH3 Buffer Data Type	W/R			
05E	SD4 Frequency HI	R	34C	CH3 Buffer Trigger Mode	W/R			
060	SD1 VLL	R	34E	CH4 Data Buffer HI Watermark	W/R			
062	SD2 VLL	R	350	CH4 Data Buffer Lo Watermark	W/R			
064	SD3 VLL	R	352	CH4 Buffer Delay Sample	W/R			
066	SD4 VLL	R	354	CH4 Buffer # of Samples	W/R			
068	SD1 REF	R	356	CH4 Buffer Sample Rate	W/R			
06A	SD2 REF	R	358	CH4 Buffer Data Type	W/R			
06C	SD3 REF	R	35A	CH4 Buffer Trigger Mode	W/R			
06E	SD4 REF	R						

Data

Date Hi Type: 16 bit unsigned integer
Date Hi & Lo Type: 24 bit unsigned integer (Multi-Speed Applications)
Range: 0 to 359.9945 degrees
Read/Write: R

For Single Speed (Ratio=1) applications, read *Data High* register of that channel. For Multi-Speed applications, read *Data High* register of the even channel (2 or 4) for that pair where 16-bit resolution is required. LSB is approximately 0.0055 degrees.

For better than 16-bit resolution Multi-Speed requirements, use *Data High* and *Data Low* registers combined to determine measured angle with up to 24-bit resolution. First read *Data High* word, then *Data Low* word. Data high word, when read, latches low word. Data Low word, when read, unlatches data. LSB is dependant upon Ratio. A gear ratio of 256 provides for a 24-bit resolution, a ratio of 128 provides for a 23-bit resolution, and so on.. The N-speed information (Multi-Speed, Fine) from the synchro should be connected to the even channel of that pair. The pairs are defined as Ch.1 & 2 and Ch.3 & 4. NOTE: Per bit angle values in below table are approximate.

DATA HIGH REGISTER																DATA LOW REGISTER															
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	.00274	.00137	.00068	.00034	.00017	.00008	.00004	.00002	X	X	X	X	X	X	X	X
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	X	X	X	X	X	X	X	X

Velocity

Type: 16 bit 2's complement word
Range: 0x7FFF maximum CW rotation to 0x8000 maximum CCW
Read/Write: R
Initialized Value: N/A

Read Velocity Registers of each channel as a 2's complement word, with 7FFFh being maximum CW rotation, and 8000h being maximum CCW rotation.

When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CW would be read as 0863h.
When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CCW would be read as F79Ch.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CW would be read as 192Ah.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CCW would be read as E6D5h.

To convert a velocity word to RPS: **Velocity in RPS = Maximum x Output / Full Scale**

If Velocity Output were E6D5h, and maximum velocity were 50.8626 RPS, then

Velocity in RPS = 50.8626 x E6D5h / 32,768 = 50.8626 x -6,442 / 32,768 = -10 RPS

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
VELOCITY	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT, 2's Complement

Ratio

Type: 16 bit unsigned integer
Range: 1 to 255
Read/Write: R/W
Initialized Value: 1 (Single-Speed)

Enter the desired ratio, as an integer number, in the *Ratio* Register corresponding to the pair of channels to be used for a two-speed, or multi-speed configuration. Example, 36:1 = integer 36. Default is for single speed applications where Ratio = 1.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RATIO	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

Angle Δ

Type: 16-bit unsigned integer
Range: 0.05 to 180 degrees
Read/Write: R/W
Initialized Value: 0

Enter the minimum differential angle to associated channel *Angle Δ* register required to trigger an angle change alert. See *Angle Δ Alert* register description for details. MSB=180°; minimum differential is 0.05°.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	approximate value
ANGLE Δ	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Degrees)

Angle Δ Initiate

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Set the bit corresponding to each channel to be monitored for angle change alert. Set bit to "1" for monitoring channels and clear bit to "0" for those not used.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE INTIATE	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL ENABLE BIT

Active Channels

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Set the bit corresponding to each channel to be monitored during BIT testing in the *Active Channel* register. Set bit to "1" for active channels and clear bit to "0" for those not used. Omitting this step will produce false alarms, because unused channels will set faults.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ACTIVE CHANNEL	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL ENABLE BIT

Latch

Type: 16 bit unsigned integer
Range: 0 or 2
Read/Write: R
Initialized Value: 0

Writing the integer 2 to the *Latch* register will cause all the channels to be latched. Reading a particular channel will disengage the latch for that channel. Writing a 0 to this register will disengage latch on all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
LATCH	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Test Angle

Type: 16-bit unsigned integer
Range: 0 to 359.9945 degrees
Read/Write: W
Initialized Value: 30°

Enter the D0 test angle as per table.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	180	90	45	22.5	11.2	5.62	2.81	1.40	.703	.352	.176	.088	.044	.022	.011	.0055	approximate value
TEST ANGLE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Degrees)

Two Speed Lock-Loss

Type: binary word
Range: N/A
Read/Write: R
Initialized Value: N/A

When two Synchros are geared to each other, either electrically or mechanically, in order to achieve higher accuracy the misalignment of the Coarse and Fine Synchros must not exceed 90°/gear ratio or the digital angle output may not be valid. Should this problem occur within a given channel pair, the corresponding bit in the *Two-Speed Lock-Loss* register will be set to "0".

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
LATCH	X	X	X	X	X	X	X	X	X	X	X	X	X	¾	X	½	CHANNEL PAIR

Velocity Scale

Type: 16 bit unsigned integer
Range: 9.5367 RPS to 152.5878 RPS
Read/Write: R/W
Initialized Value: N/A

The velocity scale factor is used to achieve a greater resolution at lower rotational speeds (RPS). The scale factor is: **4095(152.5878RPS/max RPS),** where the max RPS is selected by the user to achieve the maximum resolution for a desired RPS. Enter the scale factor as an integer to the corresponding *Velocity Scale* register for that particular channel.

To scale the Max Velocity word for 152.5878 RPS, set Velocity Scale Factor = 4095 (max velocity word of +32,767 (7FFFh) being 152.5878 RPS for CW rotation, and -32,768 (8000h) being 152.5878 RPS for CCW rotation). Scaling effects only the Velocity output word and not the dynamic performance.

To get a maximum velocity word (32,767) @ 152.5878 RPS, Scale Factor = 4095(152.5878/152.5878) = 4095 = 0FFFh;
This results in a velocity resolution of: (152.5878 RPS/32,767) x 360°/RPS = 1.676°/sec (factory default)

To get a maximum velocity word (32,767) @ 50.8626 RPS, Scale Factor = 4095(152.5878/50.8626) = 12,285 = 2FFDh);
This is a velocity resolution of: (50.8626 RPS/32,767) x 360°/RPS = 0.5588°/sec

For 9.5367 RPS max, Scale Factor = 4095(152.5878/9.5367) = 65,520 = FFF0h; 0.10477 °/sec res. (lowest setting)

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
VELOCITY SCALE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

A & B Resolution

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Individually configure encoder output resolution or commutation for each channel.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
A & B RESOLUTION	D	X	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D=DATABIT
Integer 0	0													0	0	0	16 bit Encoder Resolution
Integer 1	0													0	0	1	15 bit Encoder Resolution
Integer 2	0													0	1	0	14 bit Encoder Resolution
Integer 3	0													0	1	1	13 bit Encoder Resolution
Integer 4	0													1	0	0	12 bit Encoder Resolution
Integer 32768	1													0	0	0	4 Pole Commutation
Integer 32769	1													0	0	1	6 Pole Commutation
Integer 32770	1													0	1	0	8 Pole Commutation

Synchro / Resolver

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: N/A

Individually configure each channel for Synchro=1 or Resolver=0 measurement.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SYNCHRO / RESOLVER	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL BIT

Reference Frequency

Type: 16-bit unsigned integer
Range: 360 to 10,000 Hz
Read/Write: R/W
Initialized Value: N/A (S/R or L/R module Dependant)

Program Reference Frequency, where LSB is 1 Hz. For Example, 400 Hz = 0000 0001 1001 0000. Reference Module is Optional.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	-	8192	4096	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	approximate value
FREQUENCY	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Hz)

Reference Voltage

Type: 16-bit unsigned integer
Range: 2.0 to 28.0 Vrms
Read/Write: R/W
Initialized Value: N/A (S/R or L/R module Dependant)

Program Reference Voltage, where LSB is 0.1 Vrms. For Example, 26.1 Vrms = 0000 0001 0000 0101. Reference Module is Optional.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
	-	-	-	-	-	-	-	25.6	12.8	6.4	3.2	1.6	.8	.4	.2	.1	approximate value
VOLTAGE	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT (Vrms)

Module Design Version

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design version in ASCII. For example, ASCII "1" in upper byte and ASCII space in lower byte for Module Design Version "1 " is together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1"								ASCII " "								

Module Design Revision

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: N/A

This register holds module design revision code in ASCII. For example, ASCII "B" in upper byte and ASCII space in lower byte for Module Design Revision "B " is together 4220h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DESIGN REVISION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "B"								ASCII " "								

Module DSP

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module DSP revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE DSP	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module FPGA

Type: binary word
Range: 1 to 65535
Read/Write: R
Initialized Value: N/A

Read register as 16-bt binary word to determine Module FPGA revision. For example, 0x000B is revision 12.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE FPGA	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Module ID

Type: ASCII character (in each upper and lower byte)
Range: N/A
Read/Write: R
Initialized Value: 5331h

Read register to determine Module ID in ASCII. For example, find ASCII “S” in upper byte and ASCII “1” in lower byte, for Module “S1,” together 5331h. Slot 4 will be populated with an “S1” module for 4 or 8 channel applications. Slot 5 will be populated with an “S1” only in 8 channel applications. Slot 6 will be unused “Z0”.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII “S”								ASCII “1”								

BIT Status

Type: binary word
Range: 0 to 15
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel’s Built-In-Test (BIT) Status. Channel Status Data bit (Chn, where n is 1, 2, 3 or 4) is fail, high true, and indicates that the channel is not operating spec compliant. Status is latched. Reading any status bit will unlatch the entire register. BIT Status is part of background testing and the status register may be checked or polled at any given time.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Signal Status
Type: binary word
Range: N/A
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Signal Status. Status data bit is fail high true and indicates each a Signal input loss to that channel. Signal Loss is indicated after 2 seconds. Signal input monitoring is disabled during D3 or D0 Test. Any Signal Status failure, transient or intermittent will latch the *Signal Status* register. Reading any status bit will unlatch the entire register. Signal Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Open Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Reference Status
Type: binary word
Range: N/A
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Reference Status. Status data bit is fail high true and indicates each a Reference input loss to that channel. Signal and/or Reference Loss is indicated after 2 seconds. Signal and Reference input monitoring is disabled during D3 or D0 Test. Any Reference Status failure, transient or intermittent will latch the *Reference Status* register. Reading any status bit will unlatch the entire register. Reference Status is part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Over-Current Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
REFERENCE STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

Angle Δ Alert
Type: binary word
Range: 0 to 15
Read/Write: R
Initialized Value: 0

Check the corresponding bit for a channel's Angle Δ Alert Status. Angle Δ Alert Status Data bit (Chn, where n is 1 to 8) is fail, high true, and indicates that the angle position of that channel has exceeded the minimum differential angle specified in the *Angle Δ* register. Status is latched. Reading any status bit will unlatch the entire register. Angle Change Alert part of background testing and the status register may be checked or polled at any given time. When Status Interrupt is enabled, Status Interrupt is reported through the Max-Hi Threshold Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE Δ ALERT	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	CHANNEL STATUS BIT

BIT Status Interrupt Enable
Range: 0 to 15
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a non-compliant channel will trigger an interrupt. Default is 0 to disable all channels.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
BIT STATUS INTR ENA	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

Signal Status Interrupt Enable

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal (open) status (signal or reference input loss) will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Open Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SIGNAL STATUS INTERRUPT ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

Reference Status Interrupt Enable

Type: binary word
Range: N/A
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, a signal (open) status (signal or reference input loss) will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Over-Current Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
REFERENCE STATUS INTERRUPT ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

Angle Δ Alert Interrupt Enable

Type: binary word
Range: 0 to 15
Read/Write: R/W
Initialized Value: 0

Set the bit to enable interrupts for the corresponding channel. When enabled, an angle Δ alert will trigger an interrupt. Default is 0 to disable all channels. When Status Interrupt is enabled, Status Interrupt is reported through the Max-Hi Threshold Status Interrupt Vector in the General Use Memory Map.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
ANGLE Δ INTR ENA	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	INTERRUPT ENABLE

GENERAL USE REGISTER MEMORY MAP

The registers of this memory map apply to the complete card. The *Test Enable* and related registers affect all modules unless otherwise specified. BIT tests are module dependant. See module description for details.

MEMORY MAP

1800	Part number	R	1818	Design Version	R	1830	MAC Address HI
1802	Serial number	R	181A	Platform	R	1332	MAC Address MID
1804	Date Code	R	181C	Model	R	1834	MAC Address LO
1806	Rev. Level, PCB	R	181E	Generation	R	1836	TELNET Status
1808	Rev. Level, Processor 1	R	1820	Special Spec	R	1838	MAC Status
180A	Rev. Level, Processor 2	R	1822	Interrupt Level	R/W		
180C	Board Ready	R	1824	IP Address HI			
180E	Watchdog Timer	R/W	1826	IP Address LO			
1810	Soft reset	W	1828	Subnet Mask HI			
			182A	Subnet Mask LO			
1814	Latch All S/Ds[6]	R/W	182C	Subnet HI			
1816	(Future expansion)		182E	Subnet LO			

Address to General Use Registers has NO MODULE OFFSET.

ALL ADDRESS NOT SPECIFIED THROUGH 7FF HEX IS RESERVED.

Note: 1. Only affects A/D Modules.
2. Only affects D/A Modules.
3. Open is Signal Status for SD modules
4. Over-Current is Reference Status for SD modules
5. Max High Threshold id Angle Δ Alert for SD modules
6. Only affects S/D Modules.

Part Number

is read as a 16 bit binary word. A unique 16 bit code is assigned to each model number.

Serial Number

is read as a 16 bit binary word.

Date Code

Read as a decimal number. The four digits represent YYWW (Year, Year, Week, Week)

Revisions

Read as a 16 bit binary word

Board Ready

Poll register. Board is ready to be accessed **only after** you read “AA55”. (usually within 1 second after board power-on, but could be longer). Following a soft reset, board ready continues to indicate 0xAA55 until approx 150ms have elapsed. After that time the card is undergoing reset and the register indicates 0x0000. Following a soft reset, wait 200ms before polling Board Ready . About 1s later, the register indicates 0xAA55 which is board ready. You may proceed with read/write/coding activity after that change.

Watchdog timer

This feature monitors the watchdog timer register. When it detects that a code has been received, that code will be inverted within 100 µSec. The inverted code stays in the register until replaced by a new code. After 100 µSec. elapse, look for the inverted code to confirm that the processor is operating.

Soft reset

Soft Reset is Level sensitive. Writing a “1” initiates and holds software in reset state; then writing “0” initiates reboot (depending upon configuration, takes up to 3 seconds). This function is equivalent to a power-on reset where all parameters are reset to their default condition.

Test Enable

Set bit to enable associated Built-In Self Test D3, D2, or D0. Each test affects each Module Type differently. See the individual module section for test description(s).

Write "1" to D2 to initiate automatic background BIT testing. Card will (every 30 seconds) write 55h at *Test (D2) verification* register when D2 is enabled. User can periodically clear to 00h and then read *Test (D2) verification* register again, after 30 seconds, to verify that background bit testing is activated. D3 test cycle is completed within 45 seconds and results can be read from the associated status registers when D3 changes from "1" to "0". Any failure triggers an Interrupt (if enabled). All testing requires no external programming and is initiated by writing "1" or terminated by writing "0".

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	D0

Test (D2) Verify

Card will (every 30 seconds) write 55h at *Test (D2) Verification* register when (D2) is enabled. User can periodically clear to 00h and then read again, after 30 seconds, to verify that background bit testing is activated.

Design Version

The register holds product design version in ASCII. For example, design version 1 would be ASCII "1" is in upper byte and ASCII "space" in lower byte, together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODEL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1 "								ASCII " "								

Platform

This register holds VME platform code "64" in ASCII. Find ASCII "6" is in upper byte and ASCII "4" in lower byte, together 3634h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PLATFORM	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "6"								ASCII "4"								

Model

The register holds product model code "C " in ASCII. Find ASCII "C" is in upper byte and ASCII "space" in lower byte, together 4320h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODEL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "C "								ASCII " "								

Generation

This register holds product generation code "1 " in ASCII. Find ASCII "1" is in upper byte and ASCII "space" in lower byte, together 3120h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
GENERATION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "1"								ASCII " "								

Special Spec

This register holds product special specification code in ASCII. Find ASCII space used for none where ASCII "space" is in upper and lower bytes, together 2020h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII " "								ASCII " "								

Interrupt Levels

Write a 16-bit binary number to the *Interrupt Level Register*; 0= no interrupt; 1-7 indicates priority levels. Any fault will latch the *Status Registers* and trigger an Interrupt (if enabled.) Reading will unlatch registers. When a status bit changes before registers are read, the status change will be held in background (an interrupt is not generated) until the registers are read. After reading, registers will be updated with the background data within 250ms. The Interrupt service routine should read the associated status register to unlatch data so additional faults will trigger another Interrupt.

Interrupt Vector

Enter vector address to interrupt service routine. Write 8 bit word (0-255).

NAI ETHERNET

The 64C2 card will respond and supports TELNET Protocol. Every function that can be accessed via the VME BUS can be accessed and commanded via the Ethernet Protocol Commands.

The TELNET protocol is a call / response “set-up”. A call is made (message sent) and the card will respond.

The TELNET LOGON (LOGIN) Password (by default): NAII

The default IP address: 192.168.1.1
The default subnet: 255.255.255.0
The default gateway: 192.168.1.1

NAI Ethernet Socket Protocol, Version 1

1- This protocol applies only to card products.
2- Messaging is managed by the connected (client) computer. For version 1, the client computer will send a single message and wait for a reply from the card. Multiple cards may be managed from a single computer, subject to channel and computer capacity.

3 - Both the message and reply will be in the following format:

Preamble 2 bytes Always 5a0f	Sequence # 2 bytes	Type Code 1 byte	Size 2 bytes	Payload (0..65526 bytes)	Post-amble 2 bytes Always f0a5

4 - The Preamble and Postamble are fixed fields, intended to insure that messages are framed correctly. If either is missing the message should be ignored and the receiving device (card or computer) should either seek a new Preamble to re-establish sync, or break and re-establish the connection.

5 - The Sequence Number is a field generated by the client computer. Its value is arbitrary, but it is nominally set to an incrementing value. It will be echoed in the reply message. Its purpose is to permit the client computer to transmit multiple messages without waiting for replies, using the sequence number to correlate the replies when they do arrive

6 - The Type Code specifies the purpose of the message, which also defines the content of the payload field.

The following general rules were used to generate Type Codes:

MSB = 0 for write, 1 for read (ignored for read or write-only Type Codes)
Codes 0x00-0x0f specify system or protocol-level functions
Codes 0x10-0x7f specify card communication functions

See section labeled **Type Codes** for full list of available commands.

7 - The Size field is the value of the whole framed message including Preamble, Sequence Number, to Post-amble. For example, the register read command: “5A 0F 04 D2 10 00 0C 00 03 BC F0 A5” there are twelve bytes so the length byte is set to 0x0C

Type Codes

Type Code	Mnemonic	Function	Comments
0x00	NOP	No operation	Size is zero, board always replies NOP; useful for low-level testing
0x01	**LOG**	**Log in**	**Must be first message sent after connection is established. Payload is password. Board replies with a LOG message without the password payload, or breaks connection if password is incorrect. A LOG message with a zero payload sent by the client computer while a session in active will disconnect the session.**
0x0d	FLSH	Re-flash device	Payload to be determined
0x0e	CINFOw	Communications information write	Reserved for setting communications-related parameters
0x8e	CINFOr	Communications information read	Reserved for retrieving communications-related settings or statistical data
0x0f	NAK	Negative ACK	Sent only by the card, to indicate that a message was received that could not be interpreted. The payload may or may not contain additional information, to be defined.
0x90	**REGw (write)**	**Write to single location**	**Payload is a 24-bit address field followed by a 16-bit data field. The response is a zero-payload REGw message**
0x10	**REGr (read)**	**Read from single location**	**Payload is a 24-bit address field. The response is a REGr message with a payload containing a 24-bit address field and a 16-bit data field.**
0x91	BANKw (write)	Write to multiple locations	Payload is a 24-bit address field followed by a 16-bit count field and up to 1024 16-bit data fields. The data fields will be written into sequential card locations, beginning at the specified address. The response is a zero-payload BANKw message
0x11	BANKr (read)	Read from multiple locations	Payload is a 24-bit address field followed by a 16-bit count field. The response is a BANKr message with a payload containing a 24-bit address field followed by an 16-bit count field and up to 4095 16-bit data fields, read from sequential card locations, beginning at the specified address
0x92	MREGw (write)	Multiple write to a single location	Payload is a 24-bit address field followed by a 16-bit count field and up to 1024 16-bit data fields. The data field values will be repeatedly written into the specified card location.
0x12	MREGr (read)	Multiple read from a single location	Payload is a 24-bit address field followed by a 16-bit count field. The response is a BANKr message with a payload containing a 24-bit address field followed by a 16-bit count field and up to 4095 16-bit data fields, repeatedly read from the specified card location.
(other)	(TBD)	(TBD)	(available for expansion)

Note: The bolded **Type Codes** have been are currently being called in the VME64C2 driver.

Error Codes

In the event of an error, the board will send an error message. It will be of the same format as a standard reply with Type Code set to 0x20 and the payload will contain an Error Code.

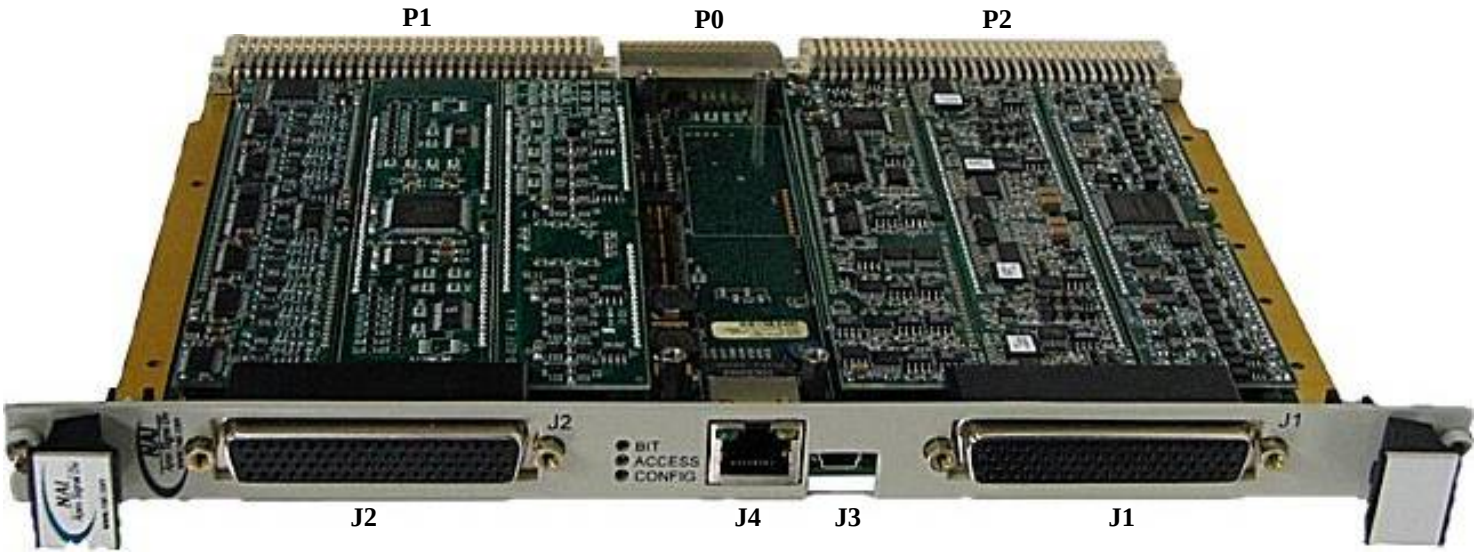
0x00 – Null event (not usually sent)
0x01 – Malformed message error - (e.g. missing preamble/post-amble)
0x02 – Incoming message buffer overflow – message lost
0x03 – Port in use
0x04 – Value in Payload out of range
0x05 – Size value in Payload (e.g. size of bank read) is incorrect
0x10 – Unknown type code error
0x11 – Address out of range error
0x12 – Address fell on odd boundary (all VME addresses must end in even numbers)
0x80 – Disconnecting port deliberately

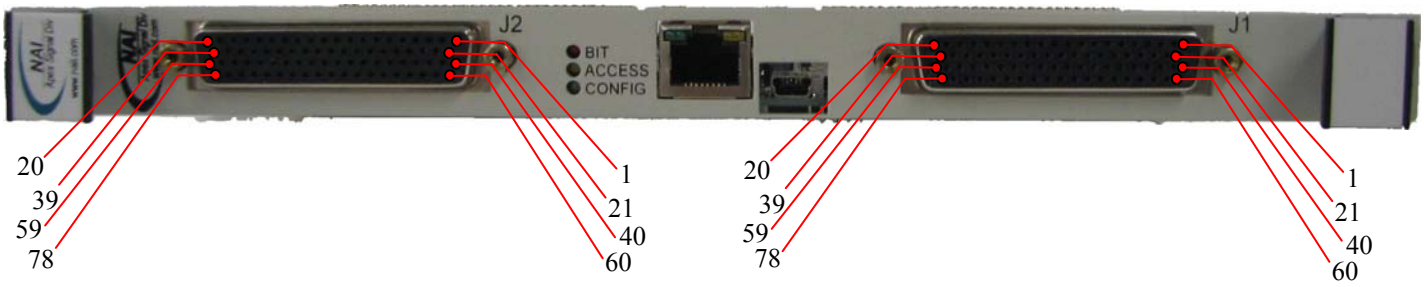
FRONT AND REAR PANEL CONNECTORS

Front Panel Connectors (78 Pin): 78-Pin D-Type Receptacle (Fem) AMP 748483-5; (Mate AMP 748368-1)
Row Z of P2, has all even-numbered pins connected to analog ground

NOTE: DO NOT CONNECT TO ANY UNDESIGNATED or (N/C) PINS

CONNECTOR PLACEMENT / DESIGNATIONS





J1, J2 Front Panel Connector - See pinout above
J3 Industry Standard USB-(Mini-B J style) (for factory use only)
J4 Industry Standard 8-pin RJ-45

SLOT 1

SLOT 1		78-pin	P2	P0	S/D	Note 4 I/O (K6)	Note 6 TTL (D7)	DIFF (D8)	REF (W1)	AD	Note 7 DA	Note 7 DA (J8)	Note 7 DA-HI-CURR	RTD (G4)	Note 8 FREQ (E5)
		J1-1	25A		S1-CH1	IO-CH1	IO-CH1	IOHI-CH1		IN1+	CH1-H	CH1-H	CH1-H	DRV+N1	
		J1-21	26A		S3-CH1	IO-CH2	IO-CH2	IOLO-CH1		IN1-	CH1-L	CH1-L	CH1-L	DRV-N1	
		J1-2	27A		S2-CH1	IO-CH3	IO-CH3	IOHI-CH2		IN2+	CH2-H		CH1-SNSH	SNS+N1	
		J1-22	28A		S4-CH1	IO-CH4	IO-CH4	IOLO-CH2		IN2-	CH2-L		CH1-SNSL	SNS-N1	
		J1-3	29A		RHI-CH1	VCC1	VCC1	IOHI-CH3	RHI-OUT	IN3+	CH3-H			DRV+N2	
		J1-23	30A		RLO-CH1	GND1	GND1	IOLO-CH3	RLO-OUT	IN3-	CH3-L			DRV-N2	
		J1-4	31A		S1-CH2	IO-CH5	IO-CH5	IOHI-CH4		IN4+	CH4-H	CH2-H	CH2-H	SNS+N2	CH1
		J1-24	32A		S3-CH2	IO-CH6	IO-CH6	IOLO-CH4		IN4-	CH4-L	CH2-L	CH2-L	SNS-N2	GND
		J1-5	25C		S2-CH2	IO-CH7	IO-CH7	IOHI-CH5		IN5+	CH5-H		CH2-SNSH	DRV+N3	
		J1-25	26C		S4-CH2	IO-CH8	IO-CH8	IOLO-CH5		IN5-	CH5-L		CH2-SNSL	DRV-N3	
		J1-6	17D		RHI-CH2	VCC2	VCC2	IOHI-CH6		GND		+VIN 1-2		SNS+N3	CH2
		J1-26	18D		RLO-CH2	GND2	GND2	IOLO-CH6				-VIN 1-2		SNS-N3	GND
		J1-40	27C		S1-CH3	IO-CH9	IO-CH9	GND		IN6+	CH6-H	CH3-H	CH3-H	DRV+N4	
		J1-60	28C		S3-CH3	IO-CH10	IO-CH10	GND		IN6-	CH6-L	CH3-L	CH3-L	DRV-N4	
		J1-41	29C		S2-CH3	IO-CH11	IO-CH11	IOHI-CH7		IN7+	CH7-H		CH3-SNSH	SNS+N4	CH3
		J1-61	30C		S4-CH3	IO-CH12	IO-CH12	IOLO-CH7		IN7-	CH7-L		CH3-SNSL	SNS-N4	GND
		J1-42	31C		RHI-CH3	VCC3	VCC3	IOHI-CH8		IN8+	CH8-H			DRV+N5	
		J1-62	32C		RLO-CH3	GND3	GND3	IOLO-CH8		IN8-	CH8-L			DRV-N5	
		J1-43	8A		S1-CH4	IO-CH13	IO-CH13	IOHI-CH9		IN9+	CH9-H	CH4-H	CH4-H	SNS+N5	CH4
		J1-63	9A		S3-CH4	IO-CH14	IO-CH14	IOLO-CH9		IN9-	CH9-L	CH4-L	CH4-L	SNS-N5	
		J1-44	10A		S2-CH4	IO-CH15	IO-CH15	IOHI-CH10		IN10+	CH10-H		CH4-SNSH	DRV+N6	GND
		J1-64	11A		S4-CH4	IO-CH16	IO-CH16	IOLO-CH10		IN10-	CH10-L		CH4-SNSL	DRV-N6	
		J1-45	19D		RHI-CH4	VCC4	VCC4	IOHI-CH11				+VIN 3-4		SNS+N6	
		J1-65	20D		RLO-CH4	GND4	GND4	IOLO-CH11				-VIN 3-4		SNS-N6	

NOTES: [1] N/A

[2] Contact Factory -- (definition of TRIG +/- (future use))

[4] I/O Module (K6) – VCC input for banks of four channels (i.e. VCC1 indicates VCC input for CH 1-4, VCC2 indicates input for CH 5-8, etc.) All GND pins are common within the module; however, each pin should be individually wired for optimal power current distribution.

[5] N/A

[6] TTL Modules -- Outputs referenced to VME GND

[7] D/A Module -- ALL D/A Low signals are connected to AGND; Common to the module, isolated from all other modules and VME GND.

[8] Freq Module -- ALL channels GND is independent per channel / module and isolated from VME GND

SLOT 2

SLOT 2		78-Pin	P2	P0	S/D	Note 4 I/O (K6)	Note 6 TTL (D7)	DIFF (D8)	REF (W1)	AD	Note 7 DA	Note 7 DA (J8)	Note 7 DA-HI-CURR	RTD G4)	Note 8 FREQ (E5)
		J1-27	12A		S1-CH1	IO-CH1	IO-CH1	IOHI-CH1		IN1+	CH1-H	CH1-H	CH1-H	DRV+N1	
		J1-8	13A		S3-CH1	IO-CH2	IO-CH2	IOLO-CH1		IN1-	CH1-L	CH1-L	CH1-L	DRV-N1	
		J1-28	14A		S2-CH1	IO-CH3	IO-CH3	IOHI-CH2		IN2+	CH2-H		CH1-SNSH	SNS+N1	
		J1-9	15A		S4-CH1	IO-CH4	IO-CH4	IOLO-CH2		IN2-	CH2-L		CH1-SNSL	SNS-N1	
		J1-29	16A		RHI-CH1	VCC1	VCC1	IOHI-CH3	RHI-OUT	IN3+	CH3-H			DRV+N2	
		J1-10	17A		RLO-CH1	GND1	GND1	IOLO-CH3	RLO-OUT	IN3-	CH3-L			DRV-N2	
		J1-30	18A		S1-CH2	IO-CH5	IO-CH5	IOHI-CH4		IN4+	CH4-H	CH2-H	CH2-H	SNS+N2	CH1
		J1-11	19A		S3-CH2	IO-CH6	IO-CH6	IOLO-CH4		IN4-	CH4-L	CH2-L	CH2-L	SNS-N2	GND
		J1-31	20A		S2-CH2	IO-CH7	IO-CH7	IOHI-CH5		IN5+	CH5-H		CH2-SNSH	DRV+N3	
		J1-12	21A		S4-CH2	IO-CH8	IO-CH8	IOLO-CH5		IN5-	CH5-L		CH2-SNSL	DRV-N3	
		J1-32	21D		RHI-CH2	VCC2	VCC2	IOHI-CH6		GND		+VIN 1-2		SNS+N3	CH2
		J1-13	22D		RLO-CH2	GND2	GND2	IOLO-CH6				-VIN 1-2		SNS-N3	GND
		J1-66	23A		S1-CH3	IO-CH9	IO-CH9	GND		IN6+	CH6-H	CH3-H	CH3-H	DRV+N4	
		J1-47	24A		S3-CH3	IO-CH10	IO-CH10	GND		IN6-	CH6-L	CH3-L	CH3-L	DRV-N4	
		J1-67	8C		S2-CH3	IO-CH11	IO-CH11	IOHI-CH7		IN7+	CH7-H		CH3-SNSH	SNS+N4	CH3
		J1-48	9C		S4-CH3	IO-CH12	IO-CH12	IOLO-CH7		IN7-	CH7-L		CH3-SNSL	SNS-N4	GND
		J1-68	10C		RHI-CH3	VCC3	VCC3	IOHI-CH8		IN8+	CH8-H			DRV+N5	
		J1-49	11C		RLO-CH3	GND3	GND3	IOLO-CH8		IN8-	CH8-L			DRV-N5	
		J1-69	12C		S1-CH4	IO-CH13	IO-CH13	IOHI-CH9		IN9+	CH9-H	CH4-H	CH4-H	SNS+N5	CH4
		J1-50	13C		S3-CH4	IO-CH14	IO-CH14	IOLO-CH9		IN9-	CH9-L	CH4-L	CH4-L	SNS-N5	
		J1-70	14C		S2-CH4	IO-CH15	IO-CH15	IOHI-CH10		IN10+	CH10-H		CH4-SNSH	DRV+N6	GND
		J1-51	15C		S4-CH4	IO-CH16	IO-CH16	IOLO-CH10		IN10-	CH10-L		CH4-SNSL	DRV-N6	
		J1-71	23D		RHI-CH4	VCC4	VCC4	IOHI-CH11				+VIN 3-4		SNS+N6	
		J1-52	24D		RLO-CH4	GND4	GND4	IOLO-CH11				-VIN 3-4		SNS-N6	

NOTES: [1] N/A

[4] I/O Module (K6) – VCC input for banks of four channels (i.e. VCC1 indicates VCC input for CH 1-4, VCC2 indicates input for CH 5-8, etc.) All GND pins are common within the module; however, each pin should be individually wired for optimal power current distribution.

[5] N/A

[6] TTL Modules -- Outputs referenced to VME GND

[7] D/A Module -- ALL D/A Low signals are connected to AGND; Common to the module, isolated from all other modules and VME GND.

[8] Freq Module -- ALL channels GND is independent per channel / module and isolated from VME GND

SLOT 3

SLOT 3		78-Pin	P2	P0	S/D	Note 4 I/O (K6)	Note 6 TTL (D7)	DIFF (D8)	REF (W1)	AD	Note 7 DA	Note 7 DA (J8)	Note 7 DA-HI-CURR	RTD G4)	Note 8 FREQ (E5)
		J1-14	1Z		S1-CH1	IO-CH1	IO-CH1	IOHI-CH1		IN1+	CH1-H	CH1-H	CH1-H	DRV+N1	
		J1-34	3Z		S3-CH1	IO-CH2	IO-CH2	IOLO-CH1		IN1-	CH1-L	CH1-L	CH1-L	DRV-N1	
		J1-15	5Z		S2-CH1	IO-CH3	IO-CH3	IOHI-CH2		IN2+	CH2-H		CH1-SNSH	SNS+N1	
		J1-35	7Z		S4-CH1	IO-CH4	IO-CH4	IOLO-CH2		IN2-	CH2-L		CH1-SNSL	SNS-N1	
		J1-16	9Z		RHI-CH1	VCC1	VCC1	IOHI-CH3	RHI-OUT	IN3+	CH3-H			DRV+N2	
		J1-36	19Z		RLO-CH1	GND1	GND1	IOLO-CH3	RLO-OUT	IN3-	CH3-L			DRV-N2	
		J1-17	11Z		S1-CH2	IO-CH5	IO-CH5	IOHI-CH4		IN4+	CH4-H	CH2-H	CH2-H	SNS+N2	CH1
		J1-37	13Z		S3-CH2	IO-CH6	IO-CH6	IOLO-CH4		IN4-	CH4-L	CH2-L	CH2-L	SNS-N2	GND
		J1-18	15Z		S2-CH2	IO-CH7	IO-CH7	IOHI-CH5		IN5+	CH5-H		CH2-SNSH	DRV+N3	
		J1-38	17Z		S4-CH2	IO-CH8	IO-CH8	IOLO-CH5		IN5-	CH5-L		CH2-SNSL	DRV-N3	
		J1-19	21Z		RHI-CH2	VCC2	VCC2	IOHI-CH6		GND		+VIN 1-2		SNS+N3	CH2
		J1-39	23Z		RLO-CH2	GND2	GND2	IOLO-CH6				-VIN 1-2		SNS-N3	GND
		J1-53		A8	S1-CH3	IO-CH9	IO-CH9	GND		IN6+	CH6-H	CH3-H	CH3-H	DRV+N4	
		J1-73		A9	S3-CH3	IO-CH10	IO-CH10	GND		IN6-	CH6-L	CH3-L	CH3-L	DRV-N4	
		J1-54		A10	S2-CH3	IO-CH11	IO-CH11	IOHI-CH7		IN7+	CH7-H		CH3-SNSH	SNS+N4	CH3
		J1-74		A11	S4-CH3	IO-CH12	IO-CH12	IOLO-CH7		IN7-	CH7-L		CH3-SNSL	SNS-N4	GND
		J1-55		A12	RHI-CH3	VCC3	VCC3	IOHI-CH8		IN8+	CH8-H			DRV+N5	
		J1-75		A17	RLO-CH3	GND3	GND3	IOLO-CH8		IN8-	CH8-L			DRV-N5	
		J1-56		A13	S1-CH4	IO-CH13	IO-CH13	IOHI-CH9		IN9+	CH9-H	CH4-H	CH4-H	SNS+N5	CH4
		J1-76		A14	S3-CH4	IO-CH14	IO-CH14	IOLO-CH9		IN9-	CH9-L	CH4-L	CH4-L	SNS-N5	
		J1-57		A15	S2-CH4	IO-CH15	IO-CH15	IOHI-CH10		IN10+	CH10-H		CH4-SNSH	DRV+N6	GND
		J1-77		A16	S4-CH4	IO-CH16	IO-CH16	IOLO-CH10		IN10-	CH10-L		CH4-SNSL	DRV-N6	
		J1-58		A18	RHI-CH4	VCC4	VCC4	IOHI-CH11				+VIN 3-4		SNS+N6	
		J1-78		A19	RLO-CH4	GND4	GND4	IOLO-CH11				-VIN 3-4		SNS-N6	
[3]REF-OUT HI			25Z												
[3]REF-OUT LO			27Z												

NOTES: [1] N/A
[3] Applies to optional On-Board Reference Module
[4] I/O Module (K6) – VCC input for banks of four channels (i.e. VCC1 indicates VCC input for CH 1-4, VCC2 indicates input for CH 5-8, etc.) All GND pins are common within the module; however, each pin should be individually wired for optimal power current distribution.
[5] N/A
[6] TTL Modules -- Outputs referenced to VME GND
[7] D/A Module -- ALL D/A Low signals are connected to AGND; Common to the module, isolated from all other modules and VME GND.
[8] Freq Module -- ALL channels GND is independent per channel / module and isolated from VME GND

SLOT 4

SLOT 4		78-Pin	P2	P0	S/D	Note 4 I/O (K6)	Note 6 TTL (D7)	DIFF (D8)	REF (W1)	AD	Note 7 DA	Note 7 DA (J8)	Note 7 DA-HI-CURR	RTD G4)	Note 8 FREQ (E5)
		J2-1	16C		S1-CH1	IO-CH1	IO-CH1	IOHI-CH1		IN1+	CH1-H	CH1-H	CH1-H	DRV+N1	
		J2-21	17C		S3-CH1	IO-CH2	IO-CH2	IOLO-CH1		IN1-	CH1-L	CH1-L	CH1-L	DRV-N1	
		J2-2	18C		S2-CH1	IO-CH3	IO-CH3	IOHI-CH2		IN2+	CH2-H		CH1-SNSH	SNS+N1	
		J2-22	19C		S4-CH1	IO-CH4	IO-CH4	IOLO-CH2		IN2-	CH2-L		CH1-SNSL	SNS-N1	
		J2-3	20C		RHI-CH1	VCC1		IOHI-CH3	RHI-OUT	IN3+	CH3-H			DRV+N2	
		J2-23	21C		RLO-CH1	GND1		IOLO-CH3	RLO-OUT	IN3-	CH3-L			DRV-N2	
		J2-4	23C		S1-CH2	IO-CH5	IO-CH5	IOHI-CH4		IN4+	CH4-H	CH2-H	CH2-H	SNS+N2	CH1
		J2-24	24C		S3-CH2	IO-CH6	IO-CH6	IOLO-CH4		IN4-	CH4-L	CH2-L	CH2-L	SNS-N2	GND
		J2-5	1A		S2-CH2	IO-CH7	IO-CH7	IOHI-CH5		IN5+	CH5-H		CH2-SNSH	DRV+N3	
		J2-25	2A		S4-CH2	IO-CH8	IO-CH8	IOLO-CH5		IN5-	CH5-L		CH2-SNSL	DRV-N3	
		J2-6	25D		RHI-CH2	VCC2		IOHI-CH6		GND		+VIN1-2		SNS+N3	CH2
		J2-26	26D		RLO-CH2	GND2		IOLO-CH6				-VIN1-2		SNS-N3	GND
		J2-40	3A		S1-CH3	IO-CH9	IO-CH9	GND		IN6+	CH6-H	CH3-H	CH3-H	DRV+N4	
		J2-60	4A		S3-CH3	IO-CH10	IO-CH10	GND		IN6-	CH6-L	CH3-L	CH3-L	DRV-N4	
		J2-41	5A		S2-CH3	IO-CH11	IO-CH11	IOHI-CH7		IN7+	CH7-H		CH3-SNSH	SNS+N4	CH3
		J2-61	6A		S4-CH3	IO-CH12	IO-CH12	IOLO-CH7		IN7-	CH7-L		CH3-SNSL	SNS-N4	GND
		J2-42	1C		RHI-CH3	VCC3		IOHI-CH8		IN8+	CH8-H			DRV+N5	
		J2-62	2C		RLO-CH3	GND3		IOLO-CH8		IN8-	CH8-L			DRV-N5	
		J2-43	3C		S1-CH4	IO-CH13	IO-CH13	IOHI-CH9		IN9+	CH9-H	CH4-H	CH4-H	SNS+N5	CH4
		J2-63	4C		S3-CH4	IO-CH14	IO-CH14	IOLO-CH9		IN9-	CH9-L	CH4-L	CH4-L	SNS-N5	
		J2-44	5C		S2-CH4	IO-CH15	IO-CH15	IOHI-CH10		IN10+	CH10-H		CH4-SNSH	DRV+N6	GND
		J2-64	6C		S4-CH4	IO-CH16	IO-CH16	IOLO-CH10		IN10-	CH10-L		CH4-SNSL	DRV-N6	
		J2-45	27D		RHI-CH4	VCC4		IOHI-CH11				+VIN3-4		SNS+N6	
		J2-65	28D		RLO-CH4	GND4		IOLO-CH11				-VIN3-4		SNS-N6	

NOTES: [1] N/A

[4] I/O Module (K6) – VCC input for banks of four channels (i.e. VCC1 indicates VCC input for CH 1-4, VCC2 indicates input for CH 5-8, etc.) All GND pins are common within the module; however, each pin should be individually wired for optimal power current distribution.

[5] N/A

[6] TTL Modules -- Outputs referenced to VME GND

[7] D/A Module -- ALL D/A Low signals are connected to AGND; Common to the module, isolated from all other modules and VME GND.

[8] Freq Module -- ALL channels GND is independent per channel / module and isolated from VME GND

SLOT 5

Slot 5		78-Pin	P2	P0	S/D	Note 4 I/O (K6)	Note 6 TTL (D7)	DIFF (D8)	REF (W1)	AD	Note 7 DA	Note 7 DA (J8)	Note 7 DA-HI-CURR	RTD G4)	Note 8 FREQ (E5)
		J2-27	7A		S1-CH1	IO-CH1	IO-CH1	IOHI-CH1		IN1+	CH1-H	CH1-H	CH1-H	DRV+N1	
		J2-8	7C		S3-CH1	IO-CH2	IO-CH2	IOLO-CH1		IN1-	CH1-L	CH1-L	CH1-L	DRV-N1	
		J2-28	22A		S2-CH1	IO-CH3	IO-CH3	IOHI-CH2		IN2+	CH2-H		CH1-SNSH	SNS+N1	
		J2-9	22C		S4-CH1	IO-CH4	IO-CH4	IOLO-CH2		IN2-	CH2-L		CH1-SNSL	SNS-N1	
		J2-29	1D		RHI-CH1	VCC1		IOHI-CH3	RHI-OUT	IN3+	CH3-H			DRV+N2	
		J2-10	2D		RLO-CH1	GND1		IOLO-CH3	RLO-OUT	IN3-	CH3-L			DRV-N2	
		J2-30	3D		S1-CH2	IO-CH5	IO-CH5	IOHI-CH4		IN4+	CH4-H	CH2-H	CH2-H	SNS+N2	CH1
		J2-11	4D		S3-CH2	IO-CH6	IO-CH6	IOLO-CH4		IN4-	CH4-L	CH2-L	CH2-L	SNS-N2	GND
		J2-31	5D		S2-CH2	IO-CH7	IO-CH7	IOHI-CH5		IN5+	CH5-H		CH2-SNSH	DRV+N3	
		J2-12	6D		S4-CH2	IO-CH8	IO-CH8	IOLO-CH5		IN5-	CH5-L		CH2-SNSL	DRV-N3	
		J2-32	29D		RHI-CH2	VCC2		IOHI-CH6		GND		+VIN1-2		SNS+N3	CH2
		J2-13	30D		RLO-CH2	GND2		IOLO-CH6				-VIN1-2		SNS-N3	GND
		J2-66	7D		S1-CH3	IO-CH9	IO-CH9	GND		IN6+	CH6-H	CH3-H	CH3-H	DRV+N4	
		J2-47	8D		S3-CH3	IO-CH10	IO-CH10	GND		IN6-	CH6-L	CH3-L	CH3-L	DRV-N4	
		J2-67	9D		S2-CH3	IO-CH11	IO-CH11	IOHI-CH7		IN7+	CH7-H		CH3-SNSH	SNS+N4	CH3
		J2-48	10D		S4-CH3	IO-CH12	IO-CH12	IOLO-CH7		IN7-	CH7-L		CH3-SNSL	SNS-N4	GND
		J2-68	11D		RHI-CH3	VCC3		IOHI-CH8		IN8+	CH8-H			DRV+N5	
		J2-49	12D		RLO-CH3	GND3		IOLO-CH8		IN8-	CH8-L			DRV-N5	
		J2-69	13D		S1-CH4	IO-CH13	IO-CH13	IOHI-CH9		IN9+	CH9-H	CH4-H	CH4-H	SNS+N5	CH4
		J2-50	14D		S3-CH4	IO-CH14	IO-CH14	IOLO-CH9		IN9-	CH9-L	CH4-L	CH4-L	SNS-N5	
		J2-70	15D		S2-CH4	IO-CH15	IO-CH15	IOHI-CH10		IN10+	CH10-H		CH4-SNSH	DRV+N6	GND
		J2-51	16D		S4-CH4	IO-CH16	IO-CH16	IOLO-CH10		IN10-	CH10-L		CH4-SNSL	DRV-N6	
		J2-71	29Z		RHI-CH4	VCC4		IOHI-CH11				+VIN3-4		SNS+N6	
		J2-52	31Z		RLO-CH4	GND4		IOLO-CH11				-VIN3-4		SNS-N6	

NOTES: [1] N/A

[4] I/O Module (K6) – VCC input for banks of four channels (i.e. VCC1 indicates VCC input for CH 1-4, VCC2 indicates input for CH 5-8, etc.) All GND pins are common within the module; however, each pin should be individually wired for optimal power current distribution.

[5] N/A

[6] TTL Modules -- Outputs referenced to VME GND

[7] D/A Module -- ALL D/A Low signals are connected to AGND; Common to the module, isolated from all other modules and VME GND.

[8] Freq Module -- ALL channels GND is independent per channel / module and isolated from VME GND

SLOT 6

Slot 6		78-Pin	P2	P0	S/D	Note 4 I/O (K6)	Note 6 TTL (D7)	DIFF (D8)	REF (W1)	AD	Note 7 DA	Note 7 DA (J8)	Note 7 DA-HI-CURR	RTD G4)	Note 8 FREQ (E5)
		J2-14		B14	S1-CH1	IO-CH1	IO-CH1	IOHI-CH1		IN1+	CH1-H	CH1-H	CH1-H	DRV+N1	
		J2-34		B15	S3-CH1	IO-CH2	IO-CH2	IOLO-CH1		IN1-	CH1-L	CH1-L	CH1-L	DRV-N1	
		J2-15		B16	S2-CH1	IO-CH3	IO-CH3	IOHI-CH2		IN2+	CH2-H		CH1-SNSH	SNS+N1	
		J2-35		B17	S4-CH1	IO-CH4	IO-CH4	IOLO-CH2		IN2-	CH2-L		CH1-SNSL	SNS-N1	
		J2-16		B18	RHI-CH1	VCC1		IOHI-CH3	RHI-OUT	IN3+	CH3-H			DRV+N2	
		J2-36		B19	RLO-CH1	GND1		IOLO-CH3	RLO-OUT	IN3-	CH3-L			DRV-N2	
		J2-17		C14	S1-CH2	IO-CH5	IO-CH5	IOHI-CH4		IN4+	CH4-H	CH2-H	CH2-H	SNS+N2	CH1
		J2-37		C15	S3-CH2	IO-CH6	IO-CH6	IOLO-CH4		IN4-	CH4-L	CH2-L	CH2-L	SNS-N2	GND
		J2-18		C16	S2-CH2	IO-CH7	IO-CH7	IOHI-CH5		IN5+	CH5-H		CH2-SNSH	DRV+N3	
		J2-38		C17	S4-CH2	IO-CH8	IO-CH8	IOLO-CH5		IN5-	CH5-L		CH2-SNSL	DRV-N3	
		J2-19		C18	RHI-CH2	VCC2		IOHI-CH6		GND		+VIN1-2		SNS+N3	CH2
		J2-39		C19	RLO-CH2	GND2		IOLO-CH6				-VIN1-2		SNS-N3	GND
		J2-53		D14	S1-CH3	IO-CH9	IO-CH9	GND		IN6+	CH6-H	CH3-H	CH3-H	DRV+N4	
		J2-73		D15	S3-CH3	IO-CH10	IO-CH10	GND		IN6-	CH6-L	CH3-L	CH3-L	DRV-N4	
		J2-54		D16	S2-CH3	IO-CH11	IO-CH11	IOHI-CH7		IN7+	CH7-H		CH3-SNSH	SNS+N4	CH3
		J2-74		D17	S4-CH3	IO-CH12	IO-CH12	IOLO-CH7		IN7-	CH7-L		CH3-SNSL	SNS-N4	GND
		J2-55		D18	RHI-CH3	VCC3		IOHI-CH8		IN8+	CH8-H			DRV+N5	
		J2-75		D19	RLO-CH3	GND3		IOLO-CH8		IN8-	CH8-L			DRV-N5	
		J2-56		E14	S1-CH4	IO-CH13	IO-CH13	IOHI-CH9		IN9+	CH9-H	CH4-H	CH4-H	SNS+N5	CH4
		J2-76		E15	S3-CH4	IO-CH14	IO-CH14	IOLO-CH9		IN9-	CH9-L	CH4-L	CH4-L	SNS-N5	
		J2-57		E16	S2-CH4	IO-CH15	IO-CH15	IOHI-CH10		IN10+	CH10-H		CH4-SNSH	DRV+N6	GND
		J2-77		E17	S4-CH4	IO-CH16	IO-CH16	IOLO-CH10		IN10-	CH10-L		CH4-SNSL	DRV-N6	
		J2-58		E18	RHI-CH4	VCC4		IOHI-CH11				+VIN3-4		SNS+N6	
		J2-78		E19	RLO-CH4	GND4		IOLO-CH11				-VIN3-4		SNS-N6	

NOTES: [1] N/A
[4] I/O Module (K6) – VCC input for banks of four channels (i.e. VCC1 indicates VCC input for CH 1-4, VCC2 indicates input for CH 5-8, etc.) All GND pins are common within the module; however, each pin should be individually wired for optimal power current distribution.
[5] N/A
[6] TTL Modules -- Outputs referenced to VME GND
[7] D/A Module -- ALL D/A Low signals are connected to AGND; Common to the module, isolated from all other modules and VME GND.
[8] Freq Module -- ALL channels GND is independent per channel / module and isolated from VME GND

Encoder/Commutation & Ethernet Connections (See Note 2 in part number section)

Encoders/Commutation are available for S/D type modules – all I/O for encoders/commutation available from P0, P2 connectors with the following limitations:

Ethernet connection is available via the front panel RJ-45 connector and the P0 rear connector (limitations for P0 Ethernet connections may occur when S/D encoders/commutation are specified)

S/D Encoder / Commutation (P0 / P2 Connector)

P0	Module 1	P0	Module 2	P0	Module 4	P2	P0	Module 5
B8	AHI-CH1	B14	AHI-CH1	A1	AHI-CH1		C5	AHI-CH1
C8	ALO-CH1	C14	ALO-CH1	A2	ALO-CH1		A6	ALO-CH1
D8	BHI-CH1	D14	BHI-CH1	A3	BHI-CH1		B6	BHI-CH1
E8	BLO-CH1	E14	BLO-CH1	A4	BLO-CH1		C6	BLO-CH1
E9	IDXHI-CH1	E15	IDXHI-CH1	A5	IDXHI-CH1		D6	IDXHI-CH1
D9	IDXLO-CH1	D15	IDXLO-CH1	B5	IDXLO-CH1		E6	IDXLO-CH1
C9	AHI-CH2	C15	AHI-CH2	B1	AHI-CH2		E7	AHI-CH2
B9	ALO-CH2	B15	ALO-CH2	B2	ALO-CH2		D7	ALO-CH2
B10	BHI-CH2	B16	BHI-CH2	B3	BHI-CH2		C7	BHI-CH2
C10	BLO-CH2	C16	BLO-CH2	B4	BLO-CH2		B7	BLO-CH2
D10	IDXHI-CH2	D16	IDXHI-CH2	C1	IDXHI-CH2		A7	IDXHI-CH2
E10	IDXLO-CH2	E16	IDXLO-CH2	C2	IDXLO-CH2		A8	IDXLO-CH2
E11	AHI-CH3	E17	AHI-CH3	D1	AHI-CH3		A9	AHI-CH3
D11	ALO-CH3	D17	ALO-CH3	D2	ALO-CH3		A10	ALO-CH3
C11	BHI-CH3	C17	BHI-CH3	D3	BHI-CH3		A11	BHI-CH3
B11	BLO-CH3	B17	BLO-CH3	D4	BLO-CH3		A12	BLO-CH3
B12	IDXHI-CH3	B18	IDXHI-CH3	D5	IDXHI-CH3		A13	IDXHI-CH3
C12	IDXLO-CH3	C18	IDXLO-CH3	E5	IDXLO-CH3		A14	IDXLO-CH3
D12	AHI-CH4	D18	AHI-CH4	E1	AHI-CH4		A15	AHI-CH4
E12	ALO-CH4	E18	ALO-CH4	E2	ALO-CH4		A16	ALO-CH4
E13	BHI-CH4	E19	BHI-CH4	E3	BHI-CH4		A17	BHI-CH4
D13	BLO-CH4	D19	BLO-CH4	E4	BLO-CH4		A18	BLO-CH4
C13	IDXHI-CH4	C19	IDXHI-CH4	C3	IDXHI-CH4	1Z		IDXHI-CH4
B13	IDXLO-CH4	B19	IDXLO-CH4	C4	IDXLO-CH4	3Z		IDXLO-CH4
No Limitation		Cannot populate M6 module		P0 Ethernet Cannot be Utilized		Cannot populate M3 module and P0 Ethernet cannot be utilized		

S/D Encoder Outputs are not available for modules installed in slots M3 and M6

Ethernet (P0 Connector)

P0	Ethernet OPTION
A1	N/C
B1	N/C
C1	N/C
D1	N/C
E1	N/C
A2	ETH-TP0 +
B2	ETH-TP0 -
C2	GND
D2	ETH-TP2 +
E2	ETH-TP2 -
A3	ETH-TP1 +
B3	ETH-TP1 -
C3	GND
D3	ETH-TP3 +
E3	ETH-TP3 -
A4	N/C
B4	N/C
C4	GND
D4	N/C
E4	N/C
A5	N/C
B5	N/C
C5	GND
D5	N/C
E5	N/C
A6	N/C
B6	N/C
C6	N/C
D6	N/C
E6	N/C
Z1-Z19	**Ground (shield)**
F1-F19	**Ground (shield)**

N/C indicates "No Connection"

NOTES: For commutation (A, B, C) outputs: A Hi becomes A, B Hi becomes B, and Index Hi becomes C.

PART NUMBER DESIGNATION

64C2 – XX XX XX XX XX XX X X X X X –XX

Slot # 1 2 3 4 5 6

MODULE (SLOT) DEFINITION

Enter Modules "A through Y" for each of Slot, 1 through 6; "Z0" if slot is not to be populated

A/D (Module C1)	Ten (10) A/D (1.25 VDC to 10.0 VDC FS) Uni or bipolar
A/D (Module C2)	Ten (10) A/D (40VDC) Uni or bipolar
A/D (Module C3)	Ten (10) 4 – 20ma Current Measurement Module
A/D (Module C4)	Ten (10) A/D (50VDC) Uni or bipolar
D/A (Module F1)	Ten (10) D/A, ±10 VDC, VME ISOLATED
D/A (Module F3)	Ten (10) D/A, ±5 VDC, VME ISOLATED
D/A (Module F5)	Four (4) D/A, ±20 VDC at 100 ma./channel max, Isolated (High current
D/A (Module J3)	Ten (10) D/A, ±1.25 VDC, VME ISOLATED
D/A (Module J5)	Ten (10) D/A, ±2.5 VDC, VME ISOLATED
D/A (Module J8)	Four (4) D/A, ±20 to ±80 VDC, VME ISOLATED
I/O TTL (Module D7)	Sixteen (16) TTL (5V System Logic Supply), Programmable for Input or Output
I/O Differential, (Module D8)	Eleven (11) Differential Multi-Mode Transceivers
I/O, Discrete, (Module K6)	Sixteen (16) Discrete (0-80V), ISOLATED, Programmable for Input or Output
LVDT (Module L*) **Note 4**	Four LVDT or RVDT-to-digital
Reference (Module W1)	One 2.2 VA programmable. 2-115 Vrms, 50 Hz-10 KHz,
RTD (Module G4)	Six (6) four-wire Platinum RTD
Signal (Module E5)	Four (4) Programmable Function Generators
S/D (Module S*) **Note 1**	Four (4) Synchro/Resolver, programmable

ON-BOARD REFERENCE MODULE (5 VA)

May be specified when slot 1 is populated with either an S/D, or LVDT or is left empty. If a second or separate reference source (W1) is required, it can use any slot. Output connection is J3-22, 44 (see slot 3 wiring)

0 = No On-Board Reference Module
1 = 2-28Vrms, 360-10kHz Programmable On-Board Reference Module
2 = Reserved for future use
3 = 115Vrms Fixed, 360-10kHz Programmable On-Board Reference Module

MECHANICAL

F = Front Panel J1, J2, and P2 & P0 I/O
S = Front Panel J1, J2, and P2 I/O (No P0)
P = P2 & P0 I/O only
G = P2 I/O only (No P0)
W = P with Wedge locks
A= VME64 Blank Front Panel and P2 & P0 I/O only
R = VME64 Blank Front Panel and P2 only (No P0)
B= VME64 Front Panel with J1, J2, P2 & P0
T VME64 Front Panel with J1, J2, P2 I/O (No P0)
D= VME64 Blank Front Panel, Low profile extractors and P2 & P0 I/O only

ENVIRONMENTAL

C = 0 TO 70
E = -40 TO +85
H = E WITH REMOVABLE COATING
K = C WITH REMOVABLE COATING

ETHERNET

0 = No Ethernet
1 = Front Panel Ethernet Connection
2 = P0 Ethernet Connection

ENCODER OUTPUTS FOR SYNCHRO / RESOLVER MODULES

0 = No Encoder outputs
1 = Encoders included for each specified Synchro module **(Note 2)**

SPECIAL OPTION CODE (OR LEAVE BLANK)

Part Number Notes:

Note 1: Synchro/Resolver four channel Measurement module selection:

(For ranges other than those listed contact factory. Customer should indicate the actual frequency applicable to his design to assure that the correct default band width is set at the factory.

	Input voltage	Reference voltage	Frequency band	
SA:	2-28 VL-L	2-115 Vrms	50-400 Hz	All Input and Reference voltages are auto ranging
SB	2-28 VL-L	2-115 Vrms	400 Hz-1 KHZ	All Input and Reference voltages are auto ranging
SC	2-28 VL-L	2-115 Vrms	1 KHZ-3 KHZ	All Input and Reference voltages are auto ranging
SD	2-28 VL-L	2-115 Vrms	3 KHZ-5 KHZ	All Input and Reference voltages are auto ranging
SE	2-28 VL-L	2-115 Vrms	5 KHZ-7 KHZ	All Input and Reference voltages are auto ranging
SF	2-28 VL-L	2-115 Vrms	7 KHZ-10 KHZ	All Input and Reference voltages are auto ranging
SG	2-28 VL-L	2-115 Vrms	10 KHZ-20 KHZ	All Input and Reference voltages are auto ranging
SH	90 VL-L	115 Vrms	50-400 Hz	Four channels
SJ	90 VL-L	115 Vrms	400 Hz- 1 KHZ	Four channels
Sx	x	x	x	Four channels defined in code table

Note 2:
Slot 1 can have encoders
Slot 2 can have encoders, but then slot 6 cannot be populated
Slot 4 can have encoders; No P0 Ethernet
Slot 5 can have encoders; but then slot 3 cannot be populated and No P0 Ethernet

Note 3: (removed)

Note 4: LVDT/RVDT four channel Measurement module selection:

(For ranges other than those listed contact factory. Customer should indicate the actual frequency applicable to his design to assure that the correct default band width is set at the factory.

LB	2-28 VL-L	2-28 Vrms	400 Hz-1 KHZ	All Input and Reference voltages are auto ranging
LC	2-28 VL-L	2-28 Vrms	1 KHZ-3 KHZ	All Input and Reference voltages are auto ranging
LD	2-28 VL-L	2-28 Vrms	3 KHZ-5 KHZ	All Input and Reference voltages are auto ranging
LE	2-28 VL-L	2-28 Vrms	5 KHZ-7 KHZ	All Input and Reference voltages are auto ranging
LF	2-28 VL-L	2-28 Vrms	7 KHZ-10 KHZ	All Input and Reference voltages are auto ranging
LG	2-28 VL-L	2-28 Vrms	10 KHZ-20 KHZ	All Input and Reference voltages are auto ranging
Lx	x	x	x	Four channels defined in code table

Revision Page

Revision	Description of Change	Engineer	Date
1.0	Initial Release. Adds Ethernet support to 64C1 rev 5.5.	GS	4/28/5
1.1	Replaces Module Special Spec with Module Design Revision. Adds Module Design Version	GS	5/9/5
1.2	Updates Ethernet connector. 64C2 has one only Ethernet port.. Following a soft reset, wait 200ms before polling Board Ready.	GS	6/8/5
1.3	Updated all Slot 6 P0 assignments and updated Encoder pin assignments.	GS	7/14/5
1.4	Updated sampling rate and group delay specifications for A/D modules C1, C2, C3, C4 (pg 7,8)	ARS	10/19/05
1.5	From K2 to K6; clarified Synchro/Resolver capabilities	FH	3/11/06
1.6	Corrected module P/N	FH	4/9/06
1.7	Added 44-pin conn pinouts, re-format	FH/as	5/16/06
1.7.2	Corrected pinouts, re-format	AS	5/23/05
1.8	Clarifications	FH	5/30/06
2.2	Formal Release; clarifications	FH/as	6/22/06
2.3	Clarifications	FH	7/9/06
2.4	Pinout corrected (slot 6); Added Ethernet Protocol (pg 77), Added A/D FIFO Buffer Operational Description (pg 24), S/D Memory Map updated	AS	7/21/06
2.5	Preliminary watermark added; Start update of A/D memory map	AS	7/27/06
2.6	Corrected A/D FIFO status register map addresses; Unit picture added; Front Panel connector pin-1 designation	AS	8/2/06
2.7	Clarified/Corrected A/D buffering, Ethernet protocol (D/A filtering in-process)	AS	10/3/06
2.8	Corrected F/J module memory registers and added Interrupt Vector	AS	10/31/06