

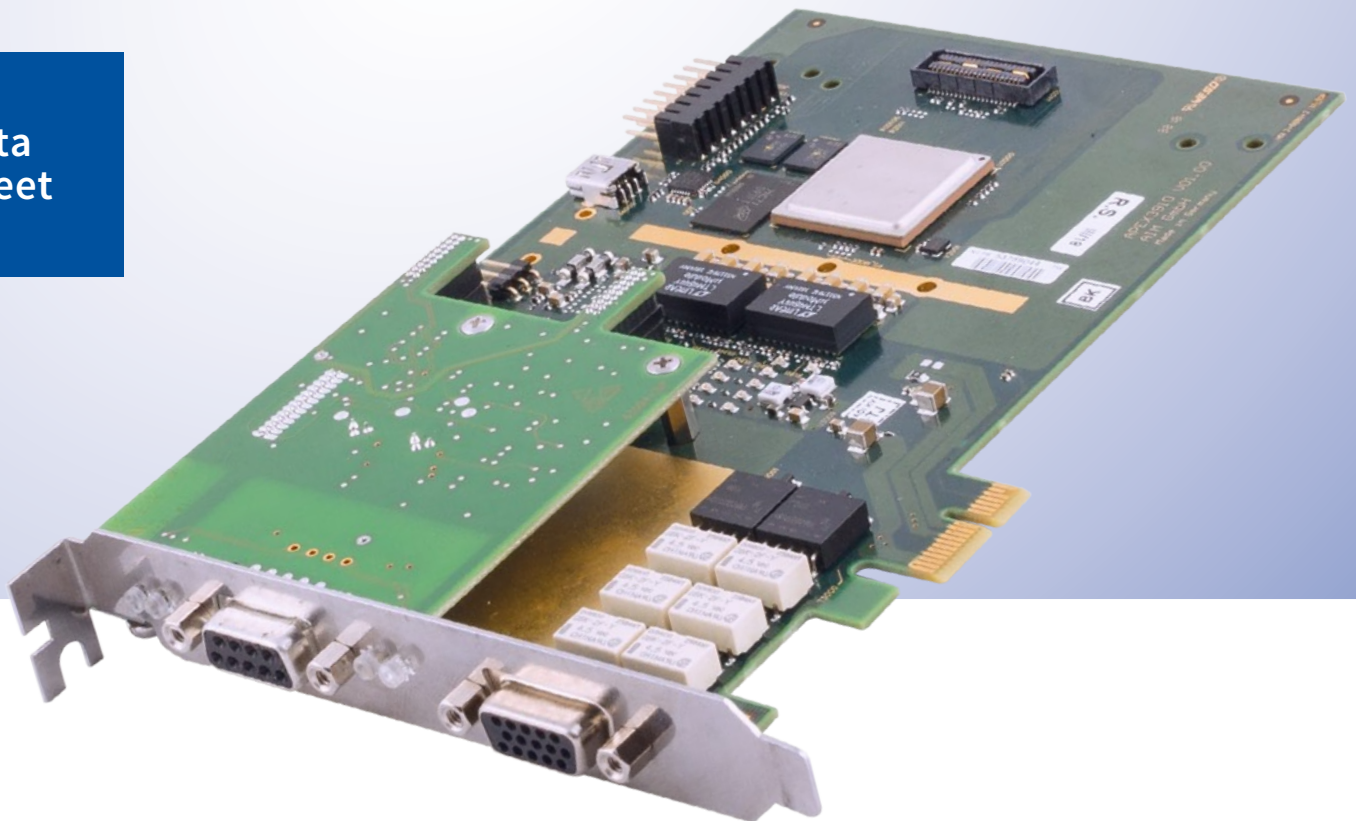


Avionics Databus  
Solutions

# APEX3910-EN

Single Stream STANAG3910  
Test & Simulation Module  
for PCI Express

Data  
Sheet



# APEX3910-EN

## Single Stream STANAG3910 Test & Simulation Module for PCI Express

### General Features

The ► **APEX3910-EN** is a member of AIM's latest family of PCI Express modules for analyzing, simulating, monitoring and testing of ► **STANAG3910** databuses. The APEX3910-EN module concurrently acts as the Bus Controller, Multiple Remote Terminals (31) and Chronological/Mailbox Bus Monitor.

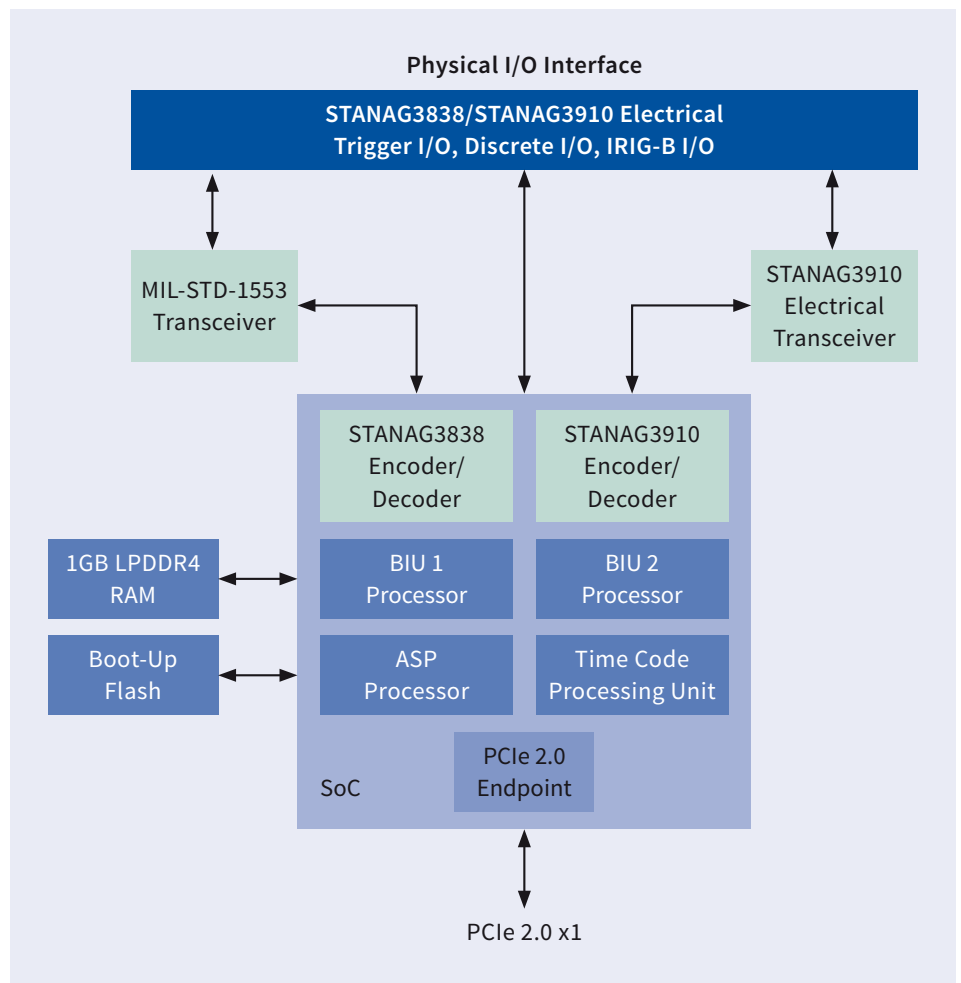
The APEX3910-EN provides 1 fully independent dual redundant STANAG3910 high speed and low speed interface on a short length PCIe x1 card form factor.

The APEX3910-EN can be used for protocol testing and simulation of STANAG3910 LS/HS Bus Controller, Multiple Remote Terminals and Chronological Monitoring at full bus loads.

All BC/RT/BM operations are performed concurrently with no degradation of performance in any operational LS/HS mode. The APEX3910-EN incorporates full protocol error injection and detection and allows the reconstruction and replay of previously recorded electrical STANAG3910 bus traffic to the LS/HS databus with excellent timing accuracy. The APEX3910-EN provides a single PCI slot solution with all the databus electrical signals accessible on a single front panel.

The APEX3910-EN card uses AIM's latest SoC (System-on-Chip) based hardware design with two dual core processing units. One dual core section is implementing the STANAG3838 and STANAG3910 Bus Interface Units (BIUs). On the second dual core section the Application Support Processor (ASP) is implemented under LINUX OS and executes the driver software onboard and minimizes the load on the host processing system.

APEX3910-EN Block Diagram



The onboard processing capabilities and a 1GB LPDDR4 RAM memory allows autonomous operation for real time applications and reduces interaction with the host processing system.

An IIRIG-B time encoder/decoder that provides both sinusoidal and a free-wheeling mode is included for time tag synchronization at the system level for single or multiple APEX3910-EN modules. The card also includes 8 Open/Ground Avionics Level (+35V) discrete I/O signals.

Full function driver software is delivered with the APEX3910-EN card in comprehensive Board Software Packages (BSPs) for Windows, LINUX and LabViewRT.

The optional ► **PBA.pro™** databus test and analysis tool (for Windows and Linux) can also be purchased for use with the APEX3910-EN card.



## Bus Controller

The APEX3910-EN provides real time Bus Controller (BC) functions for the dual redundant STANAG3910 LS/HS databus system including data buffer queues for generation of dynamic data functions for LS/HS messages.

Key Features of the Bus Controller Mode include:

- Autonomous operation including sequencing of LS Minor/Major Frames
- Acyclic Message Insertion/Deletion
- Programmable BC Retry without host Interaction
- Programmable HS Transmitter initialize Time and HS Receiver Timeout
- Full LS/HS Error Injection down to Word and Bit Level
- Multi-Buffering with Real Time Data Buffer Updates
- Synchronization of BC Operation to external Trigger Inputs
- LS Bus 4µs Inter Message Gaps

## Multiple Remote Terminal

The APEX3910-EN can simulate up to 31 LS/HS Remote Terminals with all sub-addresses each providing individually programmable Response Time. Each HS RT simulates all 128 Message Identifiers (MID). LS/HS RT's can be programmed in Mailbox Monitor mode for non-simulated RT's.

The interface provides data buffer queues allowing the generation of dynamic data functions for LS/HS messages.

Key Features of the Remote Terminal Simulation Mode include:

- Programmable Response Time for each RT with fast RT Response at 4µs
- Multi-Buffering for each simulated RT, Sub-Address and MID
- Full LS/HS Error Injection for each simulated RT, Sub-Address and MID down to Word and Bit level
- Programmable and Intelligent Response to Mode Codes
- Multi-Buffering with Real Time Data Buffer Updates

## Chronological Bus Monitor

The APEX3910-EN includes a powerful LS/HS Chronological Bus Monitor and analysis function with multiple trigger and programmable capture capabilities. Accurate time tagging of both LS and HS messages, intermessage gaps, response time and transmitter initialize time is supported.

LS/HS messages are time tagged to a 1µs resolution. LS response time and intermessage gaps as well as HS transmitter initialize time are measured down to 0.25µs.

Key Features of the Chronological Bus Monitor include:

- Multi Level Complex Sequence Trigger on:
  - LS/HS Error, LS/HS Word
  - LS/HS Data Word in Limits
- Monitor and Bus Traffic Capture:
  - 1GByte of Onboard Memory for LS/HS Messages
  - Trigger on Start, Centre and End
  - LS/HS Message Counters

## Physical Bus Replay

The APEX3910-EN module can reconstruct previously recorded STANAG3910 data bus traffic to both the LS and HS databus simultaneously with excellent timing accuracy. Recorded data files can be selected for physical bus replay.

The additional capability to disable any or all RT responses from the STANAG3910 replay enables smart systems integration and test to be performed.

## Application Support Processor

The onboard Application Support Processor (ASP) section of the APEX3910-EN offers processing functions typically provided by the host processor system.

Operational features include:

- Driver Software Execution Onboard
- Dynamic Data Generation
- Runs under LINUX Operating System

## IRIG-B Time Encoder/Decoder

APEX3910-EN modules include an onboard IRIG-B time encoder/decoder with a sinusoidal output and a free-wheeling mode for time tag synchronization. This allows synchronization of multiple APEX3910-EN or other AIM cards to one common IRIG-B time input source or to the onboard time code generator of one APEX3910-EN card as the reference for the correlation of data across multiple STANAG3910 streams.

## Physical Bus Interface

The Physical Bus Interface (PBI) including STANAG3910 HS bus Electrical Front End (EFE) and Dual Redundant STANAG3838/MIL-STD-1553B Transceiver (TRAFO) is implemented completely on a single board. Bus Interface Unit (BIU) processors support the encoder/decoder functions for STANAG3910 and STANAG3838/MIL-STD-1553A/B protocols.

The APEX3910-EN main board also supports both High Speed (HS) and MIL-STD-1553B Low Speed (LS) bus connections including a resistive terminated bus network as well as I/O connections for front panel triggering and IRIG-B signals.

Coupling to an external data bus system is software programmable.

## Trigger-/General Purpose Discrete I/O Signals

The APEX3910-EN provides BC and BM trigger inputs, BC and BM trigger outputs and 8 user programmable General Purpose Discrete I/O signals (3 on front I/O, 8 on board-to-board connector).

Voltage levels of all trigger signals and General Purpose Discrete I/O's are TTL compatible whereby the General Purpose Discrete I/O's are designed to handle avionics level as well.

## Driver Software Support

The driver software resides on the APEX3910-EN module. A full function Application Programming Interface (API) is provided compatible with 32/64-bit Windows7/8/8.1/10 and 32/64-bit LINUX.

Host applications can be written in C++, LabWindows/CVI etc. A LabView/VI application interface as well as LabViewRT drivers are provided.

## Technical Data

### Sub-System Interface

Single Lane (PCIe x1), 5Gb/s PCI Express V2.0 compliant; compatible to higher versions

### Processors

System-on-Chip Device with two Dual Core Processing sections operated at up to 1200MHz

### Memory

1GB LPDDR4 RAM

### Encoder/Decoder

STANAG3910/STANAG3838 with full error injection and detection capability

### Time Tagging

46-bit absolute IRIG-B time with 1µs resolution, sinusoidal IRIG-B output with free-wheeling mode

### Trigger I/O

BC and BM trigger input, BC and BM trigger output for LS-Bus, BM trigger output for HS-Bus (all TTL compatible)

### Discrete I/O

8 Open/Ground Avionics Level (+35V) discrete I/O

### Physical Bus Interface (PBI)

Physical Bus Interface (PBI) including STANAG3910 HS bus Electrical Front End (EFE) and MIL-STD-1553 Transceiver; Dual MIL-STD-1553B Transceiver (TRAFO) with variable output amplitude, programmable bus coupling modes with onboard terminated bus network

### Connectors

D-Sub 9-way Connector for the electrical STANAG3910 HS bus signal and STANAG3838/MIL-STD-1553B connections via high-density D-Sub 15-way connector including TTL-trigger I/O, IRIG-B time code I/O signals, 3x discrete I/O's, 16-pin ribbon cable (board-to-board) connector with 8x discrete-I/O's

### Dimensions

168mm x 107mm short length PCI format

### Power Consumption

7.5W typical @12VDC supply

### Operating Temperature Range

Standard 0°C to +45°C

Extended temperature range -15°C to +60°C

### Storage Temperature Range

-40°C to +85°C

### Humidity

0 to 95% non-condensing

## Ordering Information

### APEX3910-EN

Single stream, dual redundant PCIe x1 bus to STANAG3910 interface:

BC, Multi RT Simulator with Mailbox and Chronological Monitor, IRIG-B time encoder/decoder, 8 general purpose discrete I/O's (3 on front I/O, 8 on board-to-board connector), 1GB LPDDR4 RAM, onboard Electrical Front End (EFE)

ACB3910-HD15:

Ready made adapter cable for high density D-Sub to 2x Twinax connectors PL-75 and 1x 15-pin D-Sub connector for IRIG-B, trigger I/O and discrete I/O's

### Simulator Only version available

BC, Multi RT Simulator with Mailbox Monitor

### Single Function version available

Chronological Monitor and Mailbox Monitor OR Bus Controller OR Multi RT and Mailbox Monitor

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