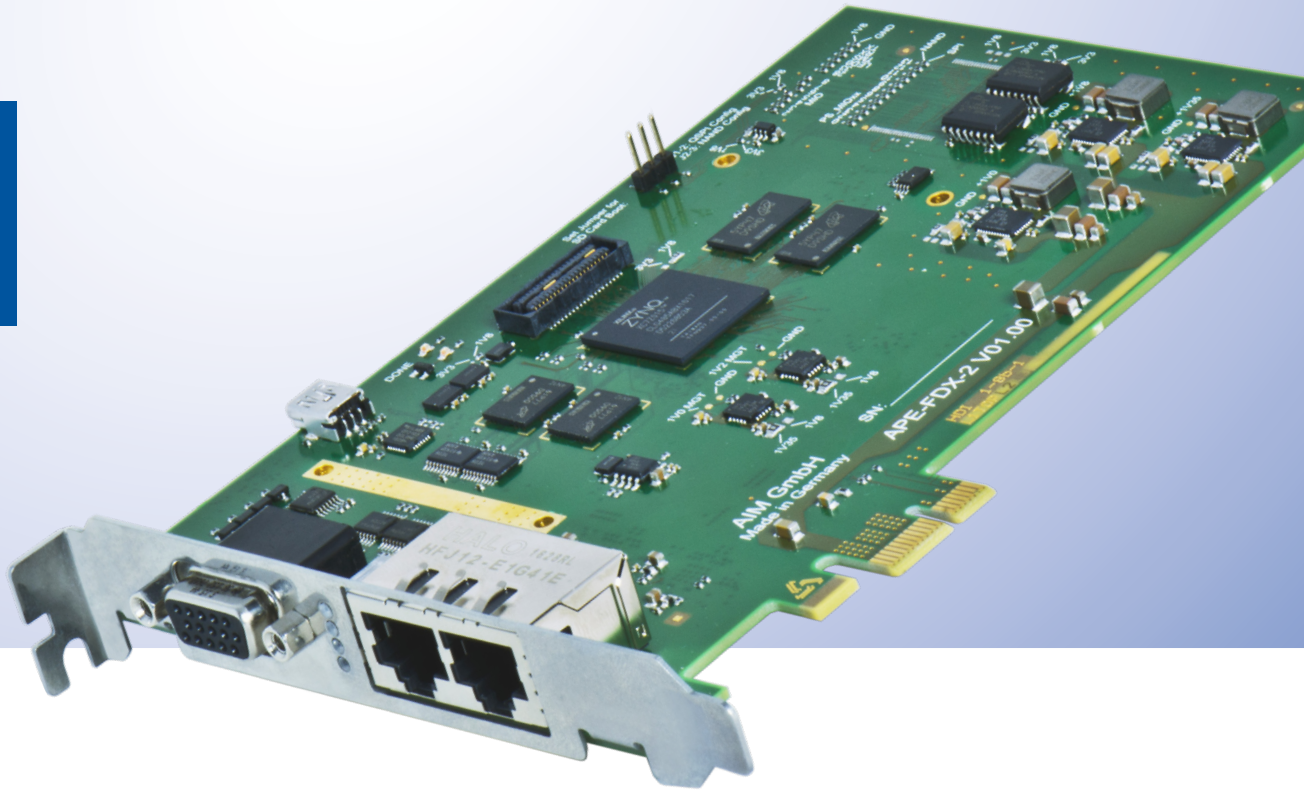
AIM
RIGHT ON TARGET

Avionics Databus Solutions

APE-FDX-2

2 Port 10/100/1000Mbit/s AFDX®/ARINC664P7 Test, Simulator and Monitor Module for PCIe

Data Sheet



www.aim-online.com

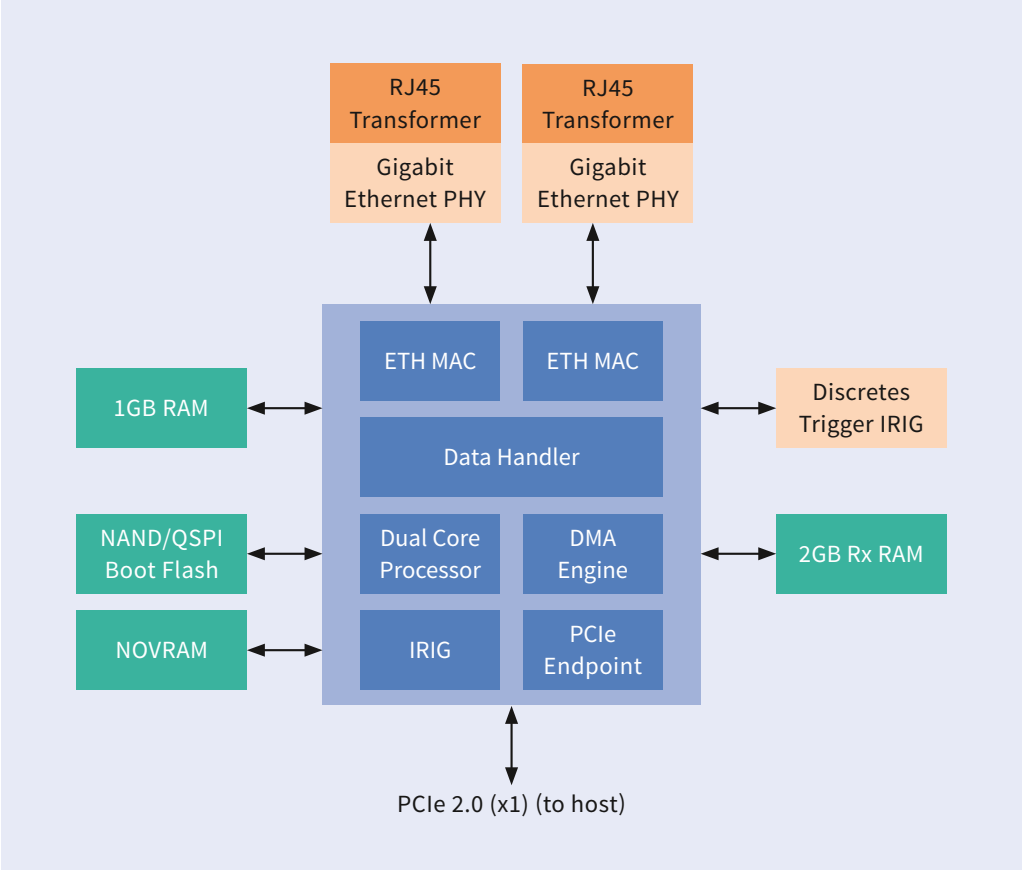
APE-FDX-2

General Features

The APE-FDX-2 is AIM's new high performance PCIe module offering full function test, simulation, monitoring and analyzer functions for AFDX®/ARINC664P7 (Avionics Full Duplex Switched Ethernet) networks. Versions available for both Airbus and Boeing variants of the ARINC664P7.
The board supports the Boeing ARINC664 extensions for EDE at the hardware interface layer with field proven real time simulation of EDE subscribers to meet all parts and multiple revisions of the EDE specifications. It's unique onboard processing capability, memory resources, customzed AFDX® MACs and IRIG-B time code decoder/generator gives AFDX® users a comprehensive feature set for the most demanding AFDX® applications.
The APE-FDX-2 PCIe module provides two AFDX®/ARINC664P7 ports being configured as two single or one dual redundant ports each implementing a 10/100/1000Mbit/s full duplex Ethernet interface. Ports can operate concurrently in traffic simulator or receiver/monitor modes with support for AFDX®/ARINC664P7 port related frame statistics.
Virtual Link (VL) packet capturing and monitoring features are complimented with powerful triggering and filtering capabilities. An integrated TAP mode enables analyzing network traffic 'in-line', with all onboard and PBA.pro features between 2 attached Ethernet devices.

The APE-FDX-2 uses AIM's field proven Common Core hardware design, utilizes a powerful System On Chip (SOC) system, integrated in a Xilinx ZYNQ® device, including programmable logic and a Dual Core processor. One processing core is acting as Bus Interface Unit (BIU) processor and the other as the Application Support Processor (ASP).
The extensive memory resources onboard allow to implement large receive buffers and complex transmit scenarios onboard.
An AFDX®/ARINC664P7 specific Physical Bus Interface implements two full duplex ports for connection to AFDX® networks.
The APE-FDX-2 module is available with the optional PBA.pro analyzer software package for Windows and Linux.

APE-FDX-2 Block Diagram

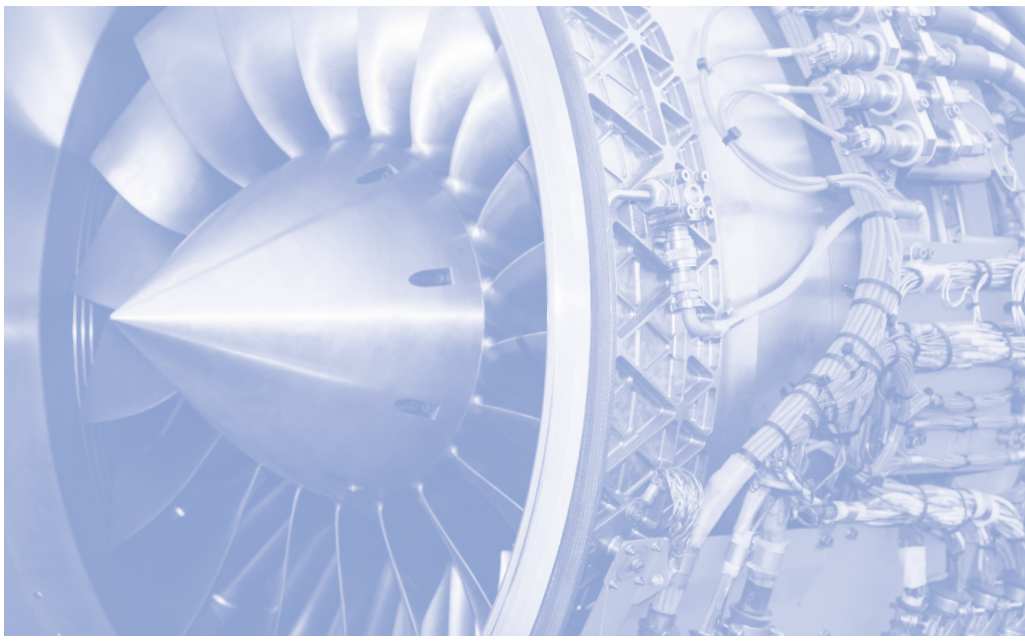


- 10/100/1000Mbit/s Ethernet compliant front end
- Xilinx ZYNQ® SOC, including Dual Core Processor
- Designed for applications such as:
  - Test & Verification of End Systems
  - Switch Testing
  - Monitoring of traffic between End Systems & Switch
  - Inter Switch Traffic Analysis
  - Multi Stream High Level System Integration
- Programmable Ports – Traffic Simulator and Receiver/Monitor Concurrently
- Synchronized Timing across Multiple Modules
- Driver software for Windows and Linux

Traffic Generation

The APE-FDX-2 provides real time traffic generation on both ports concurrently. Transmitter operation allows users to fully control all fields of the AFDX®/ARINC664P7 frame including the Virtual Link Identifier, MAC Source Address, IP Structure, UDP Structure, Payload and Sequence number. Multiple modes of transmit sequencing are supported, these being generic/replay and UDP port oriented shaped transmissions. Users can program payload data with user defined or fixed data. Inserting the time tag in the payload data provides an elegant solution to measure frame transmit delays through the network. Synchronization of transmissions across multiple ports is achieved by using strobe inputs/outputs.

- Programmable Timing & Sequencing of Frames
- Physical Error Injection – CRC, Gap, Size, Alignment
- Logical Error Injection on layers 2, 3, 4
- Timing Error Injection – Violation of Bandwidth Allocation Gap (BAG)
- Autonomous Dynamic Data Generation
- UDP Port Simulation with Traffic Shaping & Sequence Numbering
- Onboard Support for AFDX®/ARINC664P7 Sampling and Queuing Ports



UDP/VL Receive Mode

The APE-FDX-2 module ports can be configured to work in UDP/VL oriented receive mode. In this mode each UDP port has a separate buffer queue.

Received frames are stored with frame headers containing time tag and status information. Frame header information can be stored and payload data optionally discarded for the testing of switches and the complete network.
With the traffic shaping verification enabled, any violations are reported as errors in related frame headers.

- VL oriented Filtering
- Second Level Filtering on Generic Frame Parameter
- Time Stamping of Received Packets with extended IRIG-B Time Code
- Physical Error Detection, Frame Level – CRC, Gap, Size and Alignment
- AFDX®/ARINC664P7 Specific Error Detection
- Traffic Shaping Verification
- Verification of MAC, IP and UDP Headers
- VL oriented Integrity Checking

Chronological Receive Mode (Monitor Mode)

The APE-FDX-2 module ports can be configured in chronological receive mode to sequentially receive frames and store them in a circular buffer. The payload data can be discarded to optimise the use of the buffer for frame capture and analysis. Powerful filtering, triggering, complex triggering and capture modes allows users to select only the frames, data and errors of interest.

Monitor mode also provides activity monitoring and statistics for each VL recorded by the APE-FDX-2 module. The interface modules report the number of frames received and the number of errors detected globally and in VL orientated format.

- VL Orientated Receive and Filtering
- Second level filtering on Generic Frame Parameters
- Chronological Monitor with Time Stamping
- Massive onboard Monitor Buffer
- Inter Frame Gap measurements with 40ns resolution
- Comprehensive Triggering/Filtering/Capturing
- Programmable Data Capture Modes – Trace after Trigger & Recording
- Physical Error Detection – CRC, Gap, Size and Alignment
- AFDX®/ARINC664P7 Specific Error Detection

TAP Mode

The APE-FDX-2 can operate in TAP mode in all network speeds. This allows to analyze the network traffic between two attached network devices. Inter-Message-Timing will not be changed in this operational mode and network data will not be modified ensuring full operation of attached ports.

Application Support Processor

The Application Support Processor (ASP) is realized using one core SOC Processing System and provides unique on-module processing functions typically provided by host PC processing systems.

- IP and UDP layer of the AFDX®/ ARINC664P7 protocol
- Driver Software Execution on the board
- Dynamic Data Generation
- Loop/Pollution between Rx and Tx port
- Automatic Test Sequence Generation
- Linux operating systems

IRIG-B Time Code Decoder

An onboard IRIG-B Time Code decoder and generator allows synchronization of multiple AFDX®/ARINC664P7 ports using multiple APE-FDX-2 modules.
Modules can be synchronized using an external IRIG-B time source or the onboard Time code generator of one module as the reference for accurate correlation of data across multiple AFDX®/ARINC664P7 ports.

Physical Bus Interface

The APE-FDX-2 modules provide two AFDX®/ARINC664P7 ports which can be used as two single channels or as one dual redundant channel AFDX® specific Physical Bus Interface.

- Customized Media Access Controllers (MAC's) implemented in FPGA (SOC), optimised for AFDX®/ARINC664P7
- 3GByte DDR3 memory for system, receive and transmit buffer
- Physical Interface and Magnetics (COTS)
- 8-socket Network Interface connectors – RJ45
- Trigger I/O, Discrete I/O and Time Code I/O connector

Driver Software Support

The APE-FDX-2 module is supplied with an Application Programming Interface (API) and Drivers compatible with Windows and Linux.

Technical Data

Sub-System Interface
PCIe 2.0 (x1)
Processors
Dual Core Processing System, integrated in SOC Device
Memory
1GByte DDR3 Processing System RAM
2GByte DDR3 MAC Receiver RAM
Encoder/Decoder
2 AFDX®/ARINC664P7 specific Ethernet MAC's, integrated in SOC Device
- Inter Frame Gap generation and measurement with 8ns resolution (1000Mbit/s operation)

Time Tagging
46 bit absolute IRIG-B Time with 100ns resolution
Inter Frame Gap generation and measurement with 8ns resolution
Physical Bus Interface (PBI)
2 full duplex AFDX®/ARINC664P7 ports configurable to 1 dual-redundant AFDX®/ARINC664P7 port or to 1 TAP port
Connectors
- PCIe 2.0 (x1) back plane connector
- 2 x 8 way RJ45 connectors, one per AFDX®/ARINC664P7 port
- 1 x 15 way DSUB connector (female) for Time Code, Discrete I/O and Trigger I/O

Dimensions
175 x 107 mm short length Standard PCIe Format
Power Consumption
Typical 6.5W (operating)
Operating Temp. Range
Standard: 0°C to +55°C ambient
Extended: -15°C to +60°C ambient
Storage Temp. Range
-40°C to +85°C ambient
Humidity:
0 to 95% non-condensing

Ordering Information

APE-FDX-2
2 Port, PCIe 2.0 (x1) bus to 10/100/1000Mbit/s AFDX®/ARINC664P7 Interface:
Traffic Simulator, Receiver and Chronological Monitor, Integrated Tap Mode, IRIG-B Time Decoder, 3GB DDR RAM.
Includes Driver Software for Windows, LabVIEW VI's, LabVIEW RT and Linux

APE-FDX-2-G
2 Port, PCIe 2.0 (x1) bus to 10/100/1000Mbit/s AFDX®/ARINC664P7 Interface:
Generic TX/RX Function Only, Integrated Tap Mode, IRIG-B Time Decoder, 3GB DDR3 RAM.
Includes Driver Software for Windows, LabVIEW VI's, LabVIEW RT, Linux, VxWorks

APE-FDX-2-S
2 Port, PCIe 2.0 (x1) bus to 10/100/1000Mbit/s AFDX®/ARINC664P7 Interface:
Simulator TX/RX Function Only, Integrated Tap Mode, IRIG-B Time Decoder, 3GB DDR3 RAM.
Includes Driver Software for Windows, LabVIEW VI's, LabVIEW RT, Linux, VxWorks

APE-FDX-2B
2 Port, PCIe 2.0 (x1) bus to 10/100/1000Mbit/s AFDX®/ARINC664P7 Interface:
Traffic Simulator, Receiver and Chronological Monitor, Integrated Tap Mode, IRIG-B Time Decoder, 3GB DDR3 RAM.
Including Boeing EDE Specific Extensions
Includes Driver Software for Windows, LabVIEW VI's, LabVIEW RT, Linux, VxWorks

APE-FDX-2B-G
2 Port, PCIe 2.0 (x1) bus to 10/100/1000Mbit/s AFDX®/ARINC664P7 Interface:
Generic TX/RX Function Only, Integrated Tap Mode, IRIG-B Time Decoder, 3GB DDR3 RAM.
Including Boeing EDE Specific Extensions
Includes Driver Software for Windows, LabVIEW VI's, LabVIEW RT, Linux, VxWorks

APE-FDX-2B-S
2 Port, PCIe 2.0 (x1) bus to 10/100/1000Mbit/s AFDX®/ARINC664P7 Interface:
Simulator TX/RX Function Only, Integrated Tap Mode, IRIG-B Time Decoder, 3GB DDR3 RAM.
Including Boeing EDE Specific Extensions
Includes Driver Software for Windows, LabVIEW VI's, LabVIEW RT, Linux, VxWorks

Versions available for both Airbus and Boeing variants of the ARINC664P7

* AFDX® is a registered trademark of Airbus

AIM Office Contacts:

AIM GmbH
Sasbacher Str. 2
D-79111 Freiburg / Germany
Phone +49 (0)761 4 52 29-0
Fax +49 (0)761 4 52 29-33
sales@aim-online.com

AIM GmbH – Munich Sales Office
Terofalstr. 23a
D-80689 München / Germany
Phone +49 (0)89 70 92 92-92
Fax +49 (0)89 70 92 92-94
salesgermany@aim-online.com

AIM UK Office
Cressex Enterprise Centre, Lincoln Rd.
High Wycombe, Bucks. HP12 3RB / UK
Phone +44 (0)1494-446844
Fax +44 (0)1494-449324
salesuk@aim-online.com

AIM USA LLC
Seven Neshaminy Interplex
Suite 211 Trevose, PA 19053
Phone 267-982-2600
Fax 215-645-1580
salesusa@aim-online.com

APE-FDX-2_01Jun2017